CESE4130: Computer Engineering

2024-2025, lecture 2

Binary Computer Arithmetic

Computer Engineering Lab

Faculty of Electrical Engineering, Mathematics & Computer Science

2024-2025

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TU Delft

Delft University of Technology

Course objectives

- Describe number representation system and inter-conversion.
- Perform binary arithmetic operation such as addition and multiplication.
- Explain basic concepts of computer architecture.
- Use logic gates to implement simple combinational circuits.
- Explain system software and operating systems fundamentals, task management, synchronization, compilation, and interpretation.
- Use design and automation tools to perform synthesis and optimization.

Lecture objectives

- Perform binary addition and counting
- Basic Multiplication and Division Schemes

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- Understand floating point representation and operation

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- Perform binary addition and counting
- Basic Multiplication and Division Schemes
- Understand floating point representation and operation
- Familiarize with accurate and approximate operations

Overview

- Basic addition and counting
- Carry-Lookahead adders

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- Basic addition and counting
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- Basic multiplication operation
- Basic division operation

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- Basic multiplication operation
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- Floating point representation
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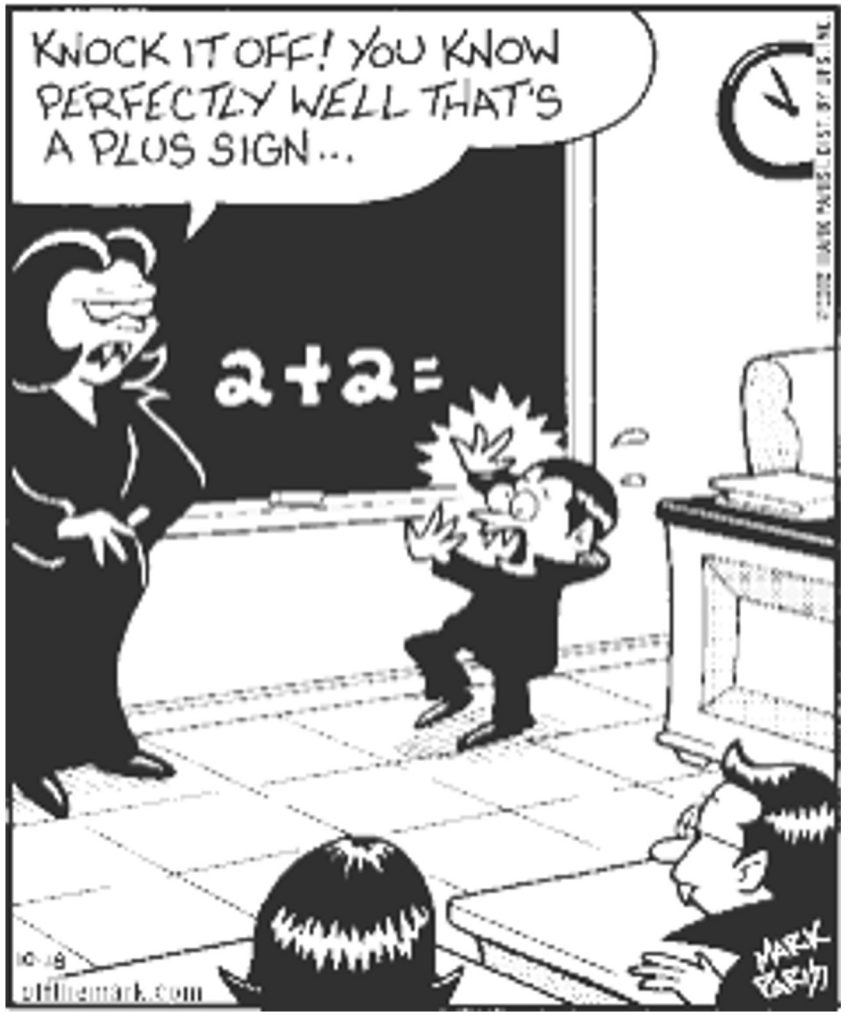
- Basic addition and counting
- Carry-Lookahead adders
- Basic multiplication operation
- Basic division operation
- Floating point representation
- Floating point operation
- Advanced cases

Basic addition and counting

Computers know only 1’s and 0’s



Basic addition and counting

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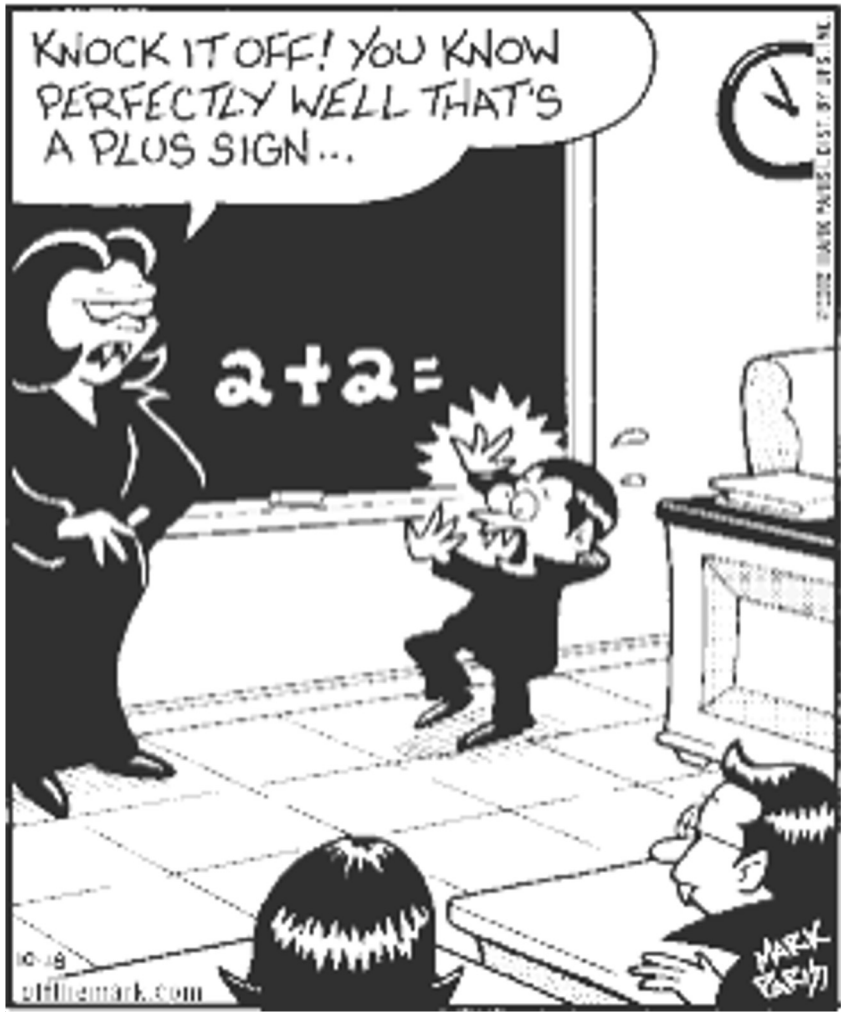

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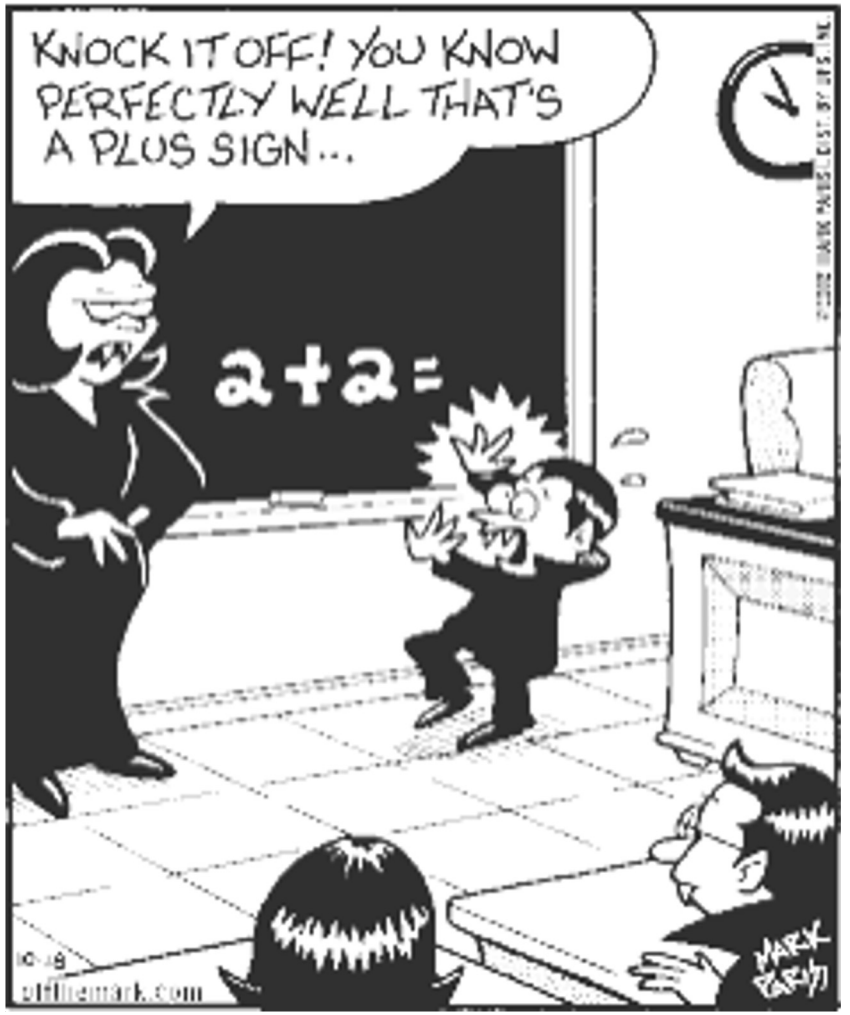
- Same principles of adding normal decimals



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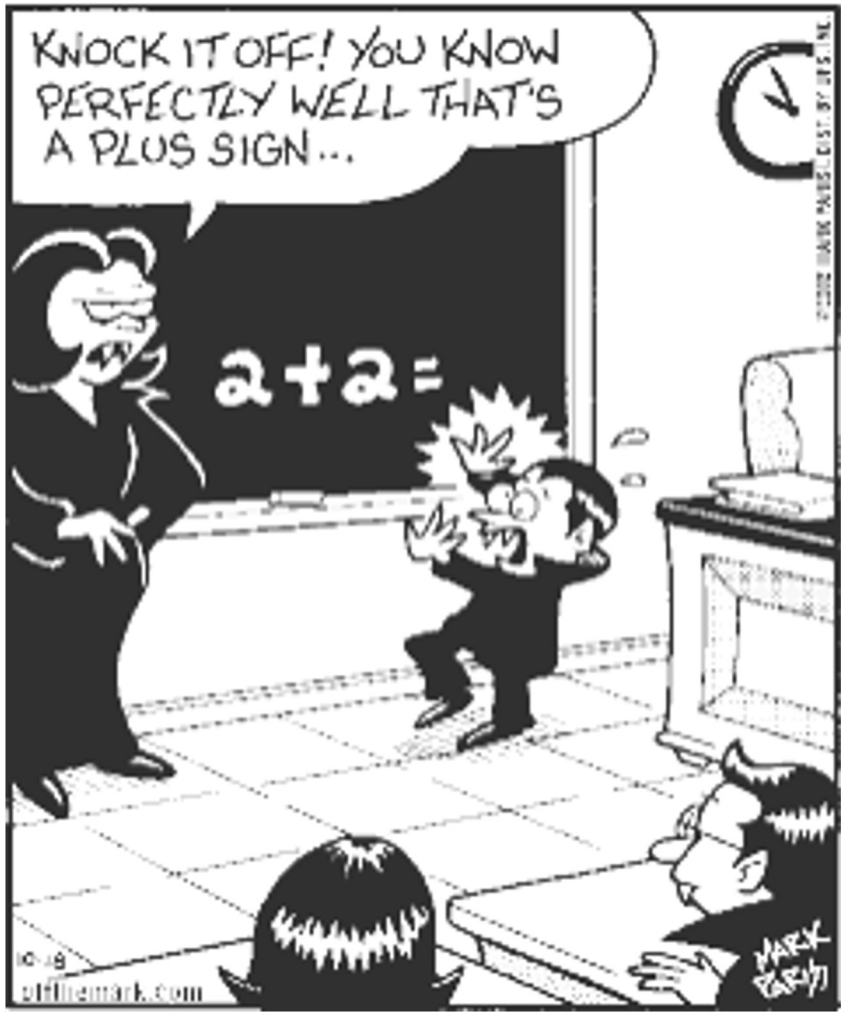

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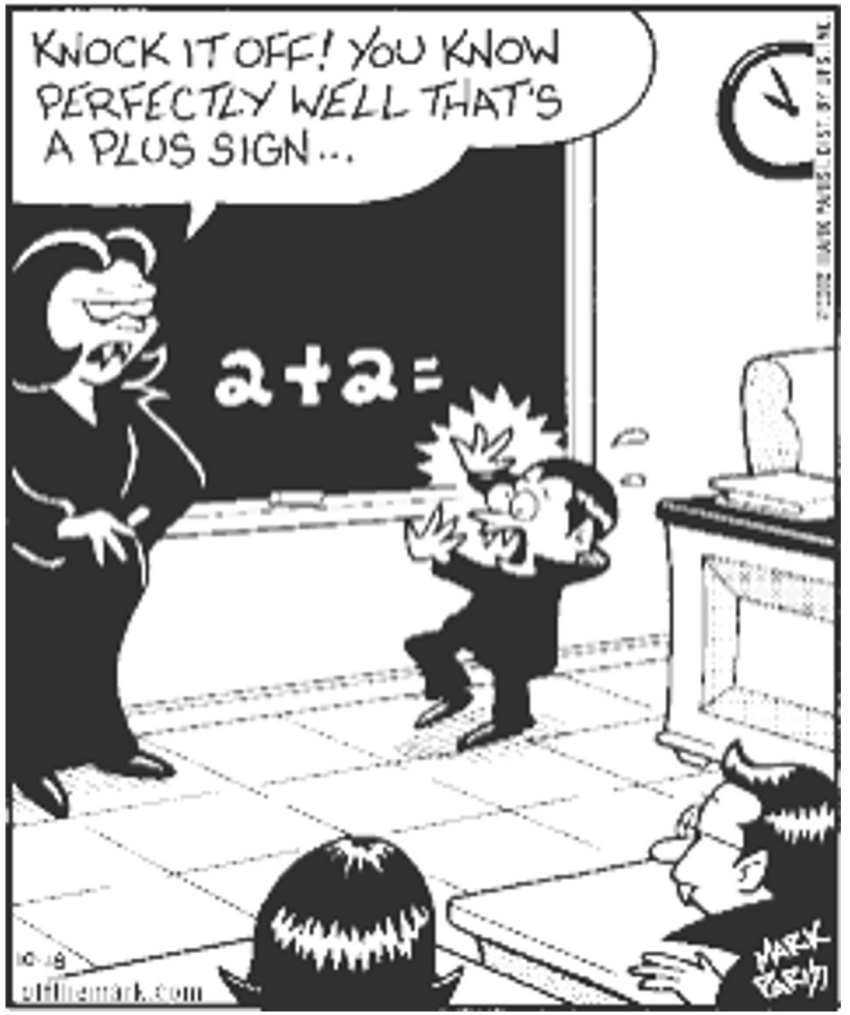
Fundamental rules of binary addition

- 0 + 0 = 0



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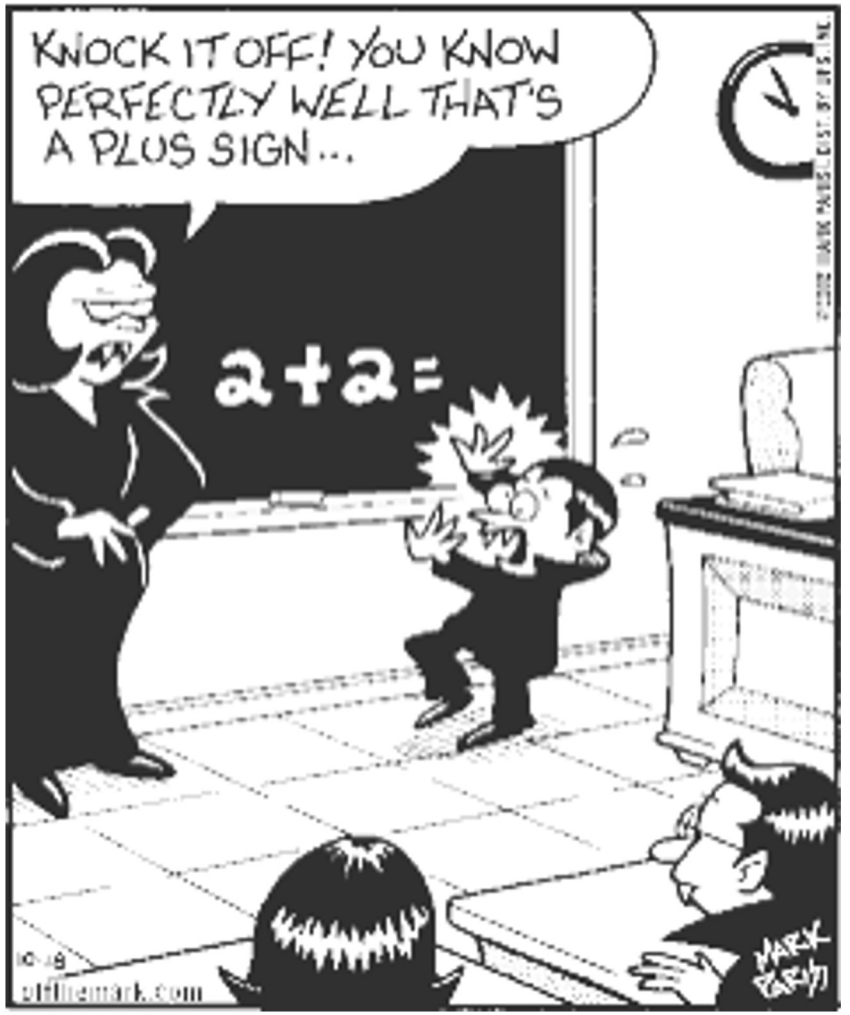

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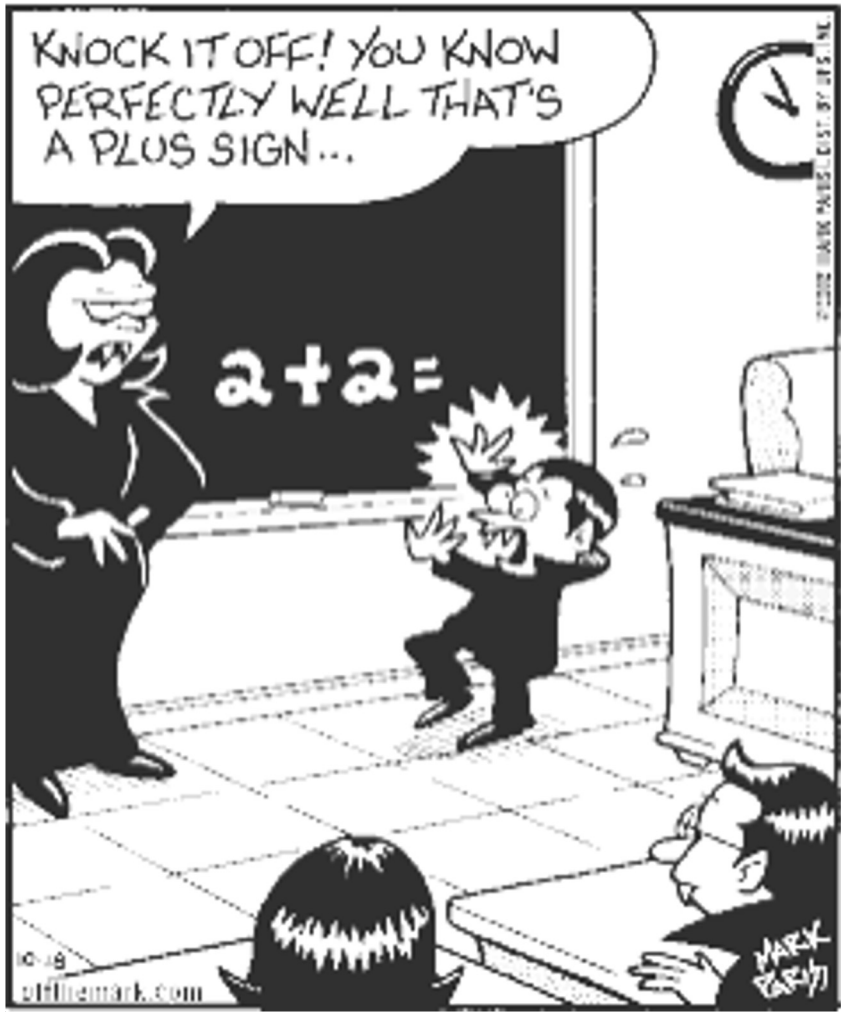

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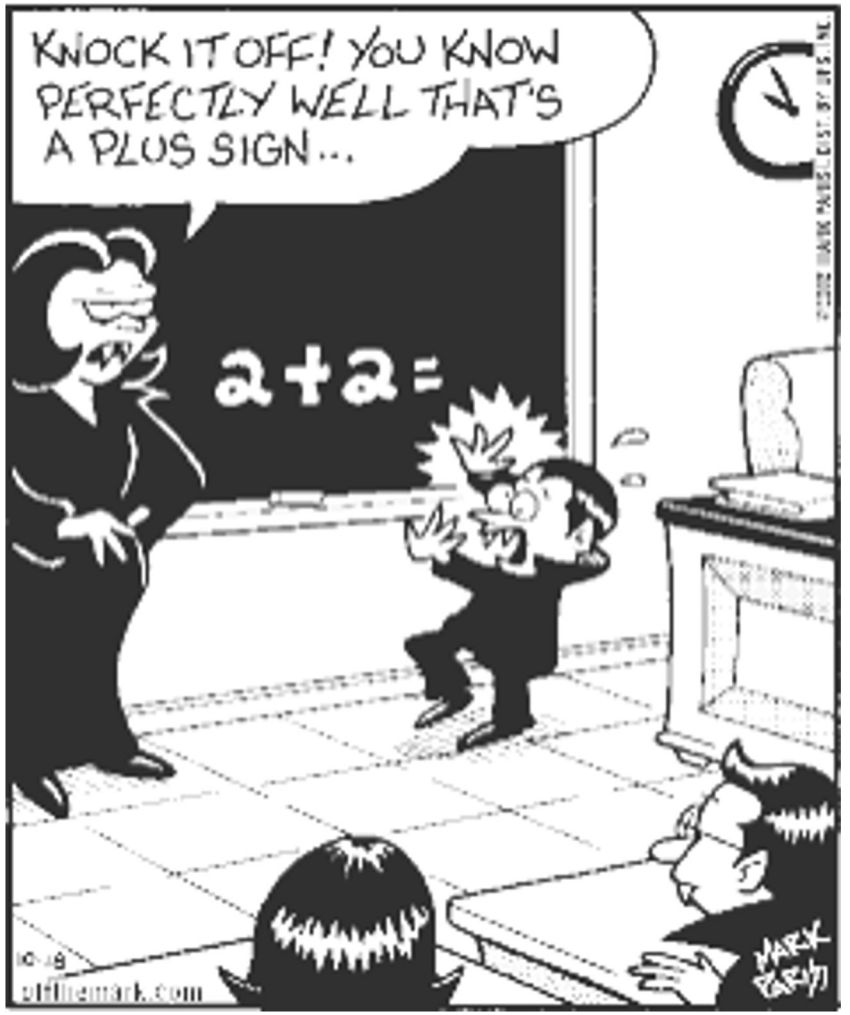
Consider

Why do we use the "carry" method?



Binary addition

- Decimal addition is simple:

Binary addition

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```
  8
+7
=
```

Binary addition

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```
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15

Binary addition

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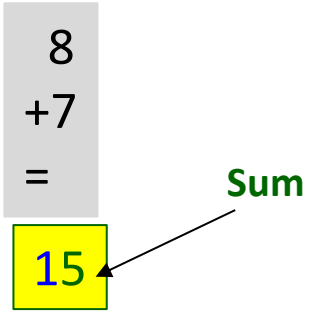

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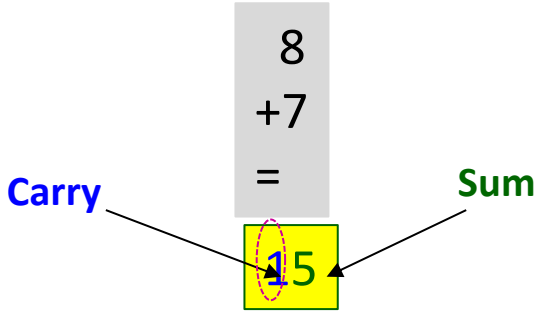

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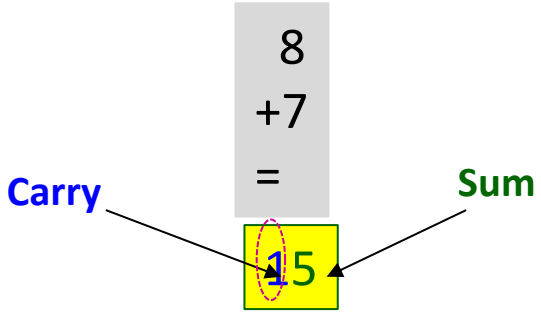

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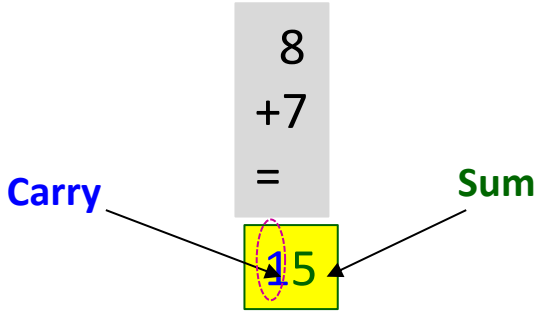

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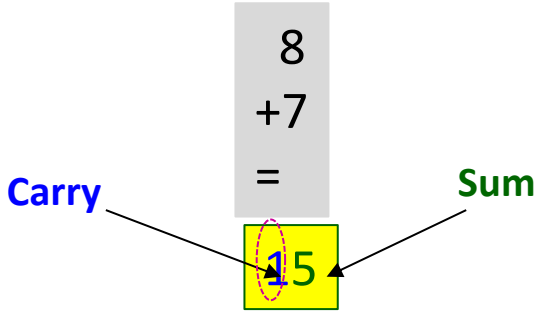

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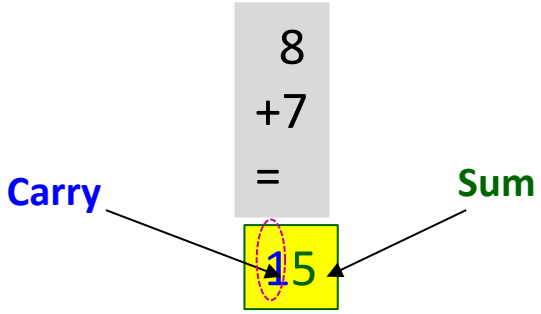

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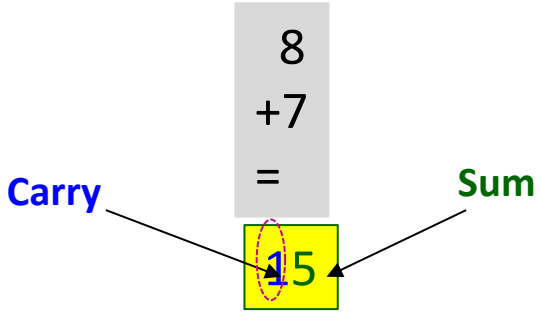

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Sum

Carry

Binary addition

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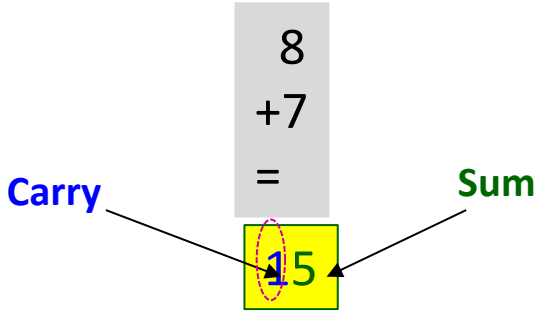

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- It requires 2 outputs to represent sum and carry

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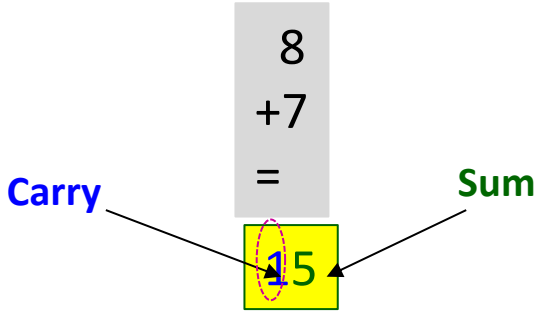

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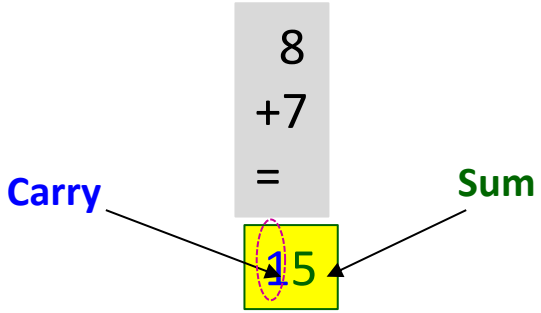

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A= 0110 (6) & B=1011 (11)

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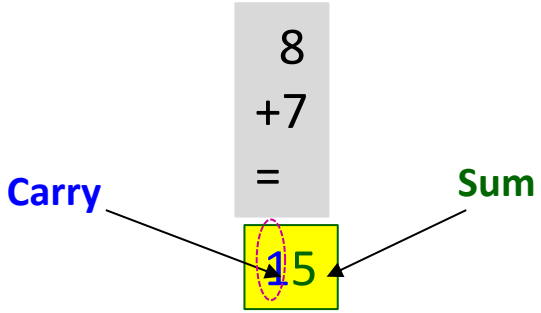

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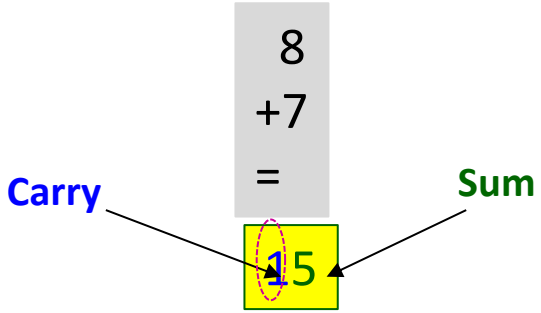

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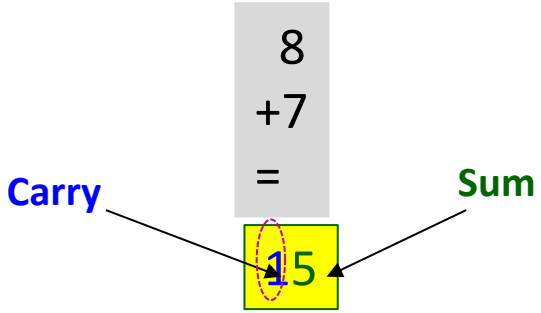

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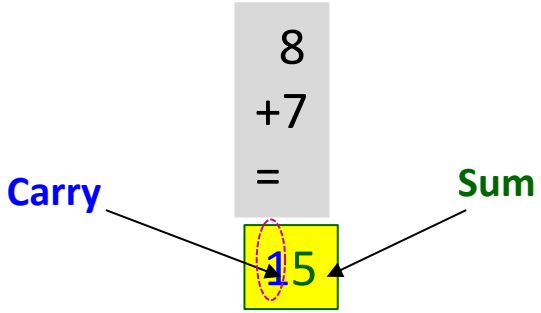

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```
        1 0
Carry   ^^
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        ------
Sum       01
```

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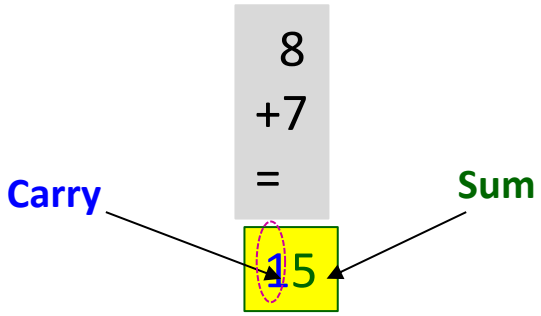

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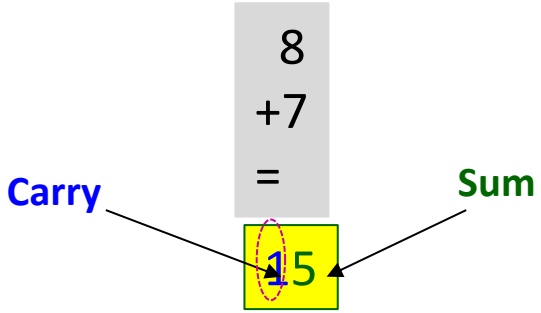

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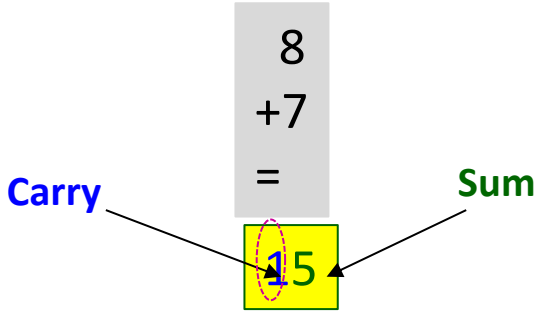

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Addition result = 10001 (17)

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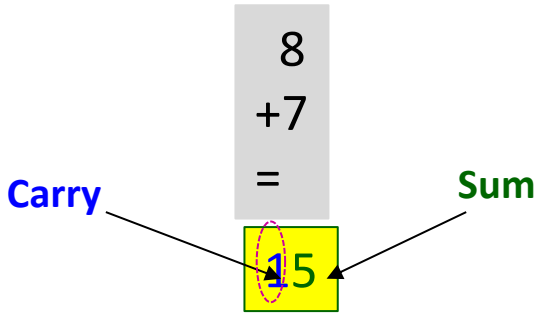

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- How can it be implemented?

Basic addition and counting

How are the fundamental addition rules implemented in hardware?

Half Adder

Basic addition and counting

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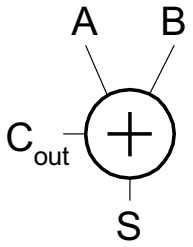
Half Adder

- Two 1-bit inputs
- Two 1-bit outputs



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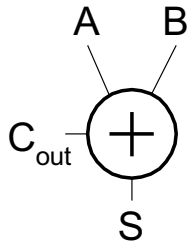
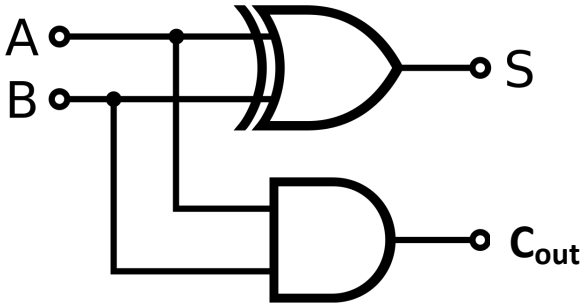


$$S = A \oplus B$$

$$C_{out} = A \bullet B$$



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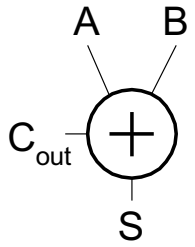

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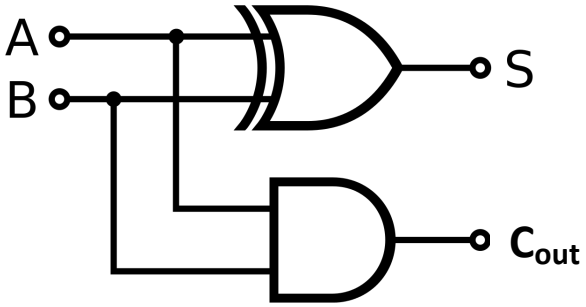

What happens when there is a third/carry input?

Basic addition and counting

How are the fundamental addition rules implemented in hardware?

Half Adder

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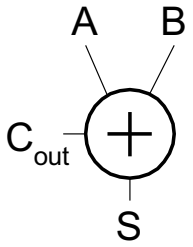

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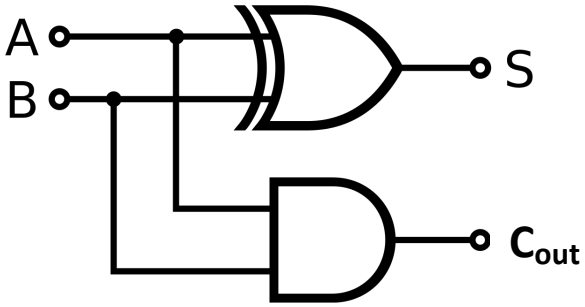
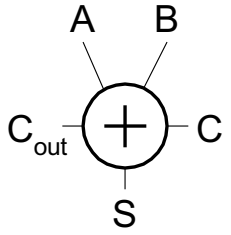


Full Adder

- Three 1-bit inputs
- Two 1-bit outputs



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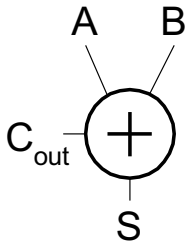

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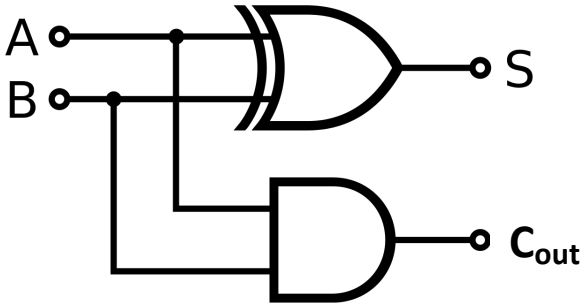

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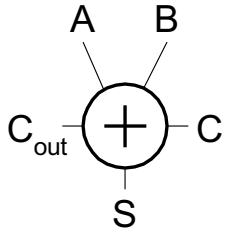
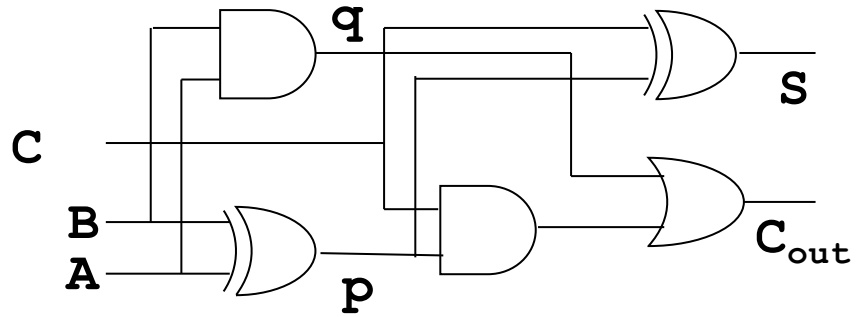


$$S = A \oplus B \oplus C$$

$$C_{out} = MAJ(A, B, C)$$



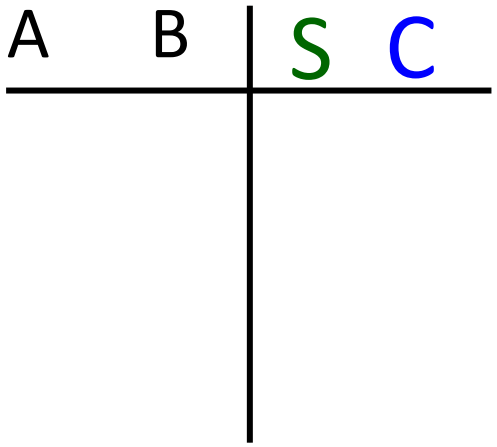
What happens when there is a third/carry input?

Simple adder design: half adder

- Performs 1-bit addition

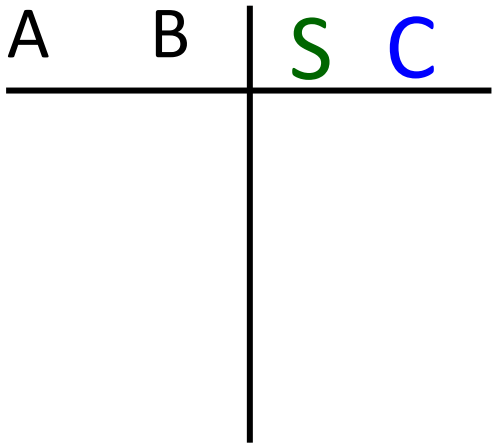
Simple adder design: half adder

- Performs 1-bit addition
  - Inputs: A, B, Outputs: S, C



Simple adder design: half adder

- Performs 1-bit addition
  - Inputs: A, B, Outputs: S, C
  - Generate truth table



Simple adder design: half adder

- Performs 1-bit addition
  - Inputs: A, B, Outputs: S, C
  - Generate truth table

A	B	S	C
0	0	0	0
0	1	1	0

Simple adder design: half adder

- Performs 1-bit addition
  - Inputs: A, B, Outputs: S, C
  - Generate truth table

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Simple adder design: half adder

- Performs 1-bit addition
  - Inputs: A, B, Outputs: S, C
  - Generate truth table
- Extract Boolean expression

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Simple adder design: half adder

- Performs 1-bit addition
  - Inputs: A, B, Outputs: S, C
  - Generate truth table
- Extract Boolean expression
  - Using K-map

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Simple adder design: half adder

- Performs 1-bit addition
  - Inputs: A, B, Outputs: S, C
  - Generate truth table
- Extract Boolean expression
  - Using K-map

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Simple adder design: half adder

- Performs 1-bit addition
  - Inputs: A, B, Outputs: S, C
  - Generate truth table
- Extract Boolean expression
  - Using K-map

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

$S = \bar{A}B + A\bar{B}$

Simple adder design: half adder

- Performs 1-bit addition
  - Inputs: A, B, Outputs: S, C
  - Generate truth table
- Extract Boolean expression
  - Using K-map

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

$S = \bar{A}B + A\bar{B}$

$S = A \oplus B$

Simple adder design: half adder

- Performs 1-bit addition
  - Inputs: A, B, Outputs: S, C
  - Generate truth table
- Extract Boolean expression
  - Using K-map

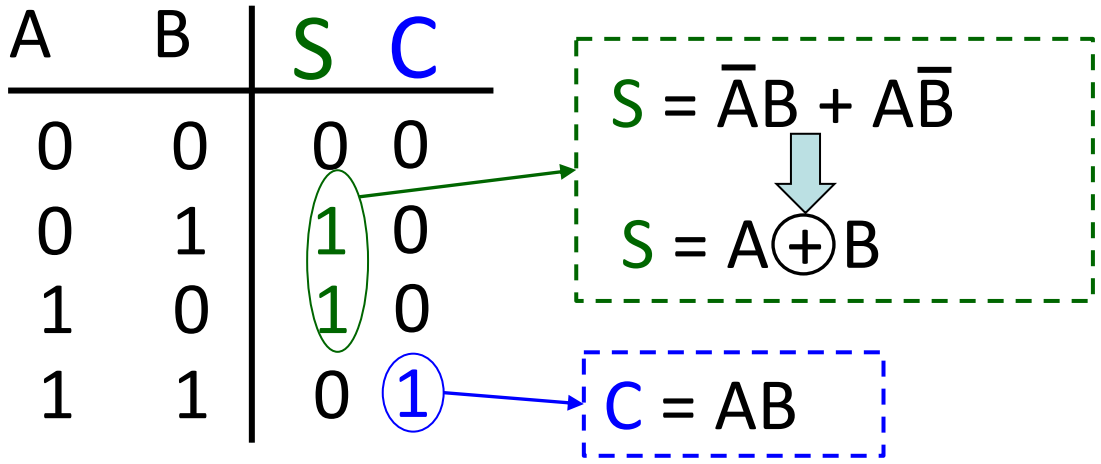
A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

$S = \bar{A}B + A\bar{B}$

$S = A \oplus B$

Simple adder design: half adder

- Performs 1-bit addition
  - Inputs: A, B, Outputs: S, C
  - Generate truth table
- Extract Boolean expression
  - Using K-map



Simple adder design: half adder

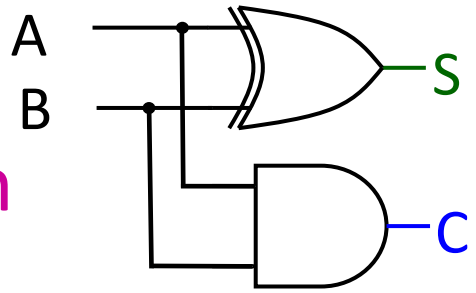
- Performs 1-bit addition
  - Inputs: A, B, Outputs: S, C
  - Generate truth table
- Extract Boolean expression
  - Using K-map
- Implement the Boolean expression with logic gates

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

$S = \bar{A}B + A\bar{B}$

$S = A \oplus B$

$C = AB$



Simple adder design: half adder

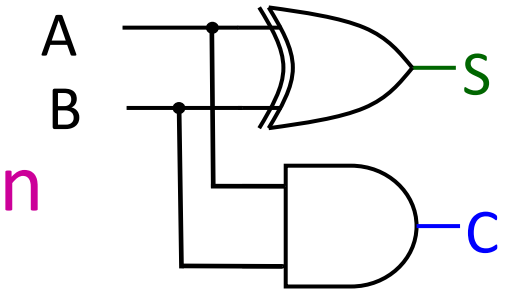
- Performs 1-bit addition
  - Inputs: A, B, Outputs: S, C
  - Generate truth table
- Extract Boolean expression
  - Using K-map
- Implement the Boolean expression with logic gates
- Half adder block diagram

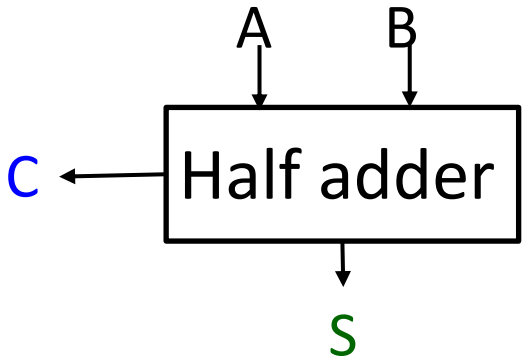
A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

$S = \bar{A}B + A\bar{B}$

$S = A \oplus B$

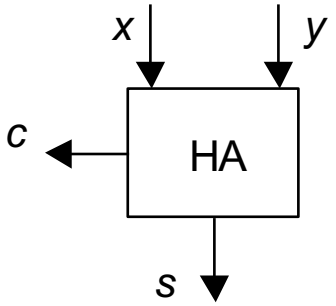
$C = AB$





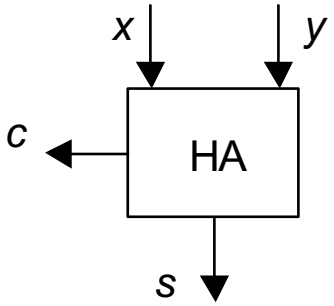
Half adder implementations

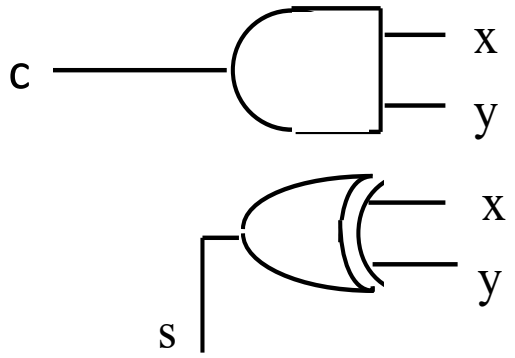
Inputs		Outputs	
x	*y*	*c*	*s*
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0



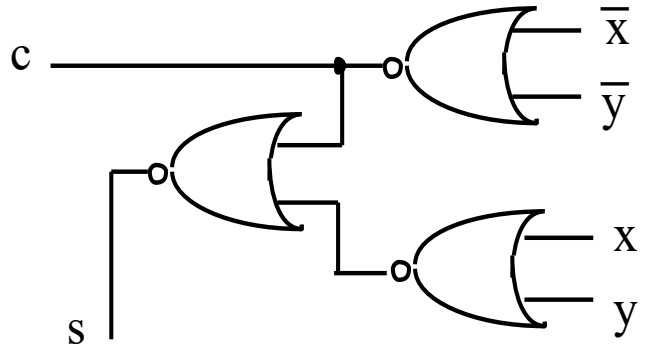
Half adder implementations

Inputs		Outputs	
x	*y*	*c*	*s*
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

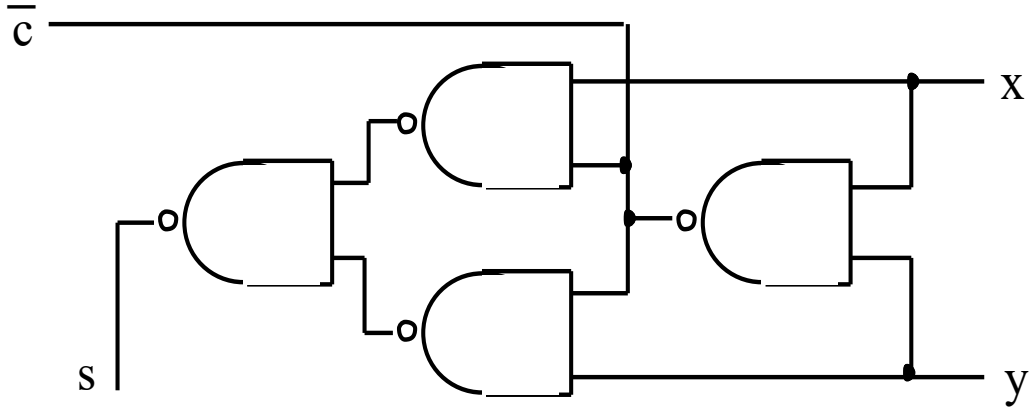




(a) AND/XOR half-adder.



(b) NOR-gate half-adder.



(c) NAND-gate half-adder with complemented carry.

Simple adder design: full adder

- Adds three 1-bit inputs

Simple adder design: full adder

- Adds three 1-bit inputs
  - Inputs: A_i, B_i, C_i
  - Outputs: S_o, C_o

A_i B_i C_i	S_o C_o

Simple adder design: full adder

- Adds three 1-bit inputs
  - Inputs: A_i, B_i, C_i
  - Outputs: S_o, C_o
- Generate truth table

A_i	B_i	C_i	S_o	C_o
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Simple adder design: full adder

- Adds three 1-bit inputs
  - Inputs: A_i, B_i, C_i
  - Outputs: S_o, C_o
- Generate truth table

A_i	B_i	C_i	S_o	C_o
0	0	0	0	0
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Simple adder design: full adder

- Adds three 1-bit inputs
  - Inputs: A_i, B_i, C_i
  - Outputs: S_o, C_o
- Generate truth table

A_i	B_i	C_i	S_o	C_o
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1		
1	0	0	1	0
1	0	1		
1	1	0		
1	1	1		

Simple adder design: full adder

- Adds three 1-bit inputs
  - Inputs: A_i, B_i, C_i
  - Outputs: S_o, C_o
- Generate truth table

A_i	B_i	C_i	S_o	C_o
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1		

Simple adder design: full adder

- Adds three 1-bit inputs
  - Inputs: A_i, B_i, C_i
  - Outputs: S_o, C_o
- Generate truth table

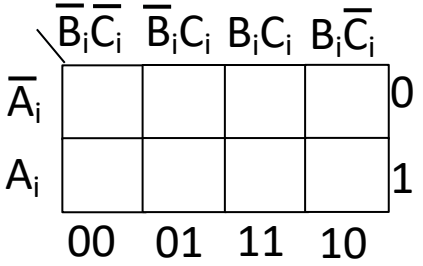
A_i	B_i	C_i	S_o	C_o
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Simple adder design: full adder

- Adds three 1-bit inputs
  - Inputs: A_i, B_i, C_i
  - Outputs: S_o, C_o
- Generate truth table
- Extract Boolean expressions
  - Using K-map

A_i	B_i	C_i	S_o	C_o
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

K-map for S_o



Simple adder design: full adder

- Adds three 1-bit inputs
  - Inputs: A_i, B_i, C_i
  - Outputs: S_o, C_o
- Generate truth table
- Extract Boolean expressions
  - Using K-map

A_i	B_i	C_i	S_o	C_o
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

K-map for S_o

A_i \ B_iC_i	$\overline{B}_i\overline{C}_i$	$\overline{B}_iC_i$	B_iC_i	$B_i\overline{C}_i$
$\overline{A}_i$		1		1
A_i	1		1	

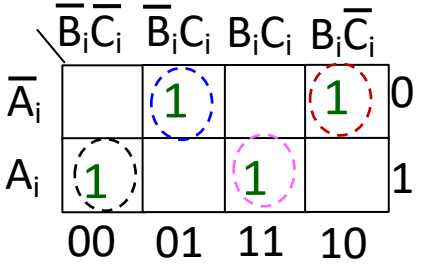
00 01 11 10

Simple adder design: full adder

- Adds three 1-bit inputs
  - Inputs: A_i, B_i, C_i
  - Outputs: S_o, C_o
- Generate truth table
- Extract Boolean expressions
  - Using K-map

A_i	B_i	C_i	S_o	C_o
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

K-map for S_o

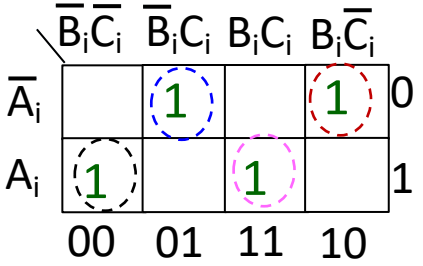


Simple adder design: full adder

- Adds three 1-bit inputs
  - Inputs: A_i, B_i, C_i
  - Outputs: S_o, C_o
- Generate truth table
- Extract Boolean expressions
  - Using K-map

A_i	B_i	C_i	S_o	C_o
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

K-map for S_o



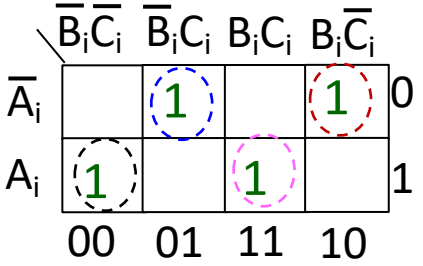
$S_o = \overline{A}_i\overline{B}_iC_i + \overline{A}_iB_i\overline{C}_i + A_i\overline{B}_i\overline{C}_i + A_iB_iC_i$

Simple adder design: full adder

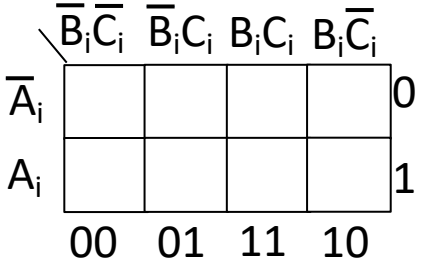
- Adds three 1-bit inputs
  - Inputs: A_i, B_i, C_i
  - Outputs: S_o, C_o
- Generate truth table
- Extract Boolean expressions
  - Using K-map

A_i	B_i	C_i	S_o	C_o
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

K-map for S_o



K-map for C_o



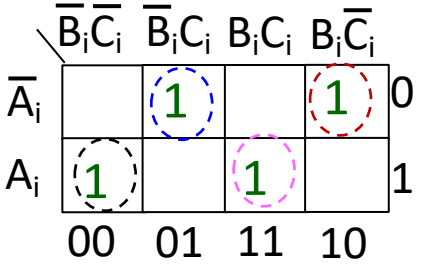
$S_o = \overline{A}_i\overline{B}_iC_i + \overline{A}_iB_i\overline{C}_i + A_i\overline{B}_i\overline{C}_i + A_iB_iC_i$

Simple adder design: full adder

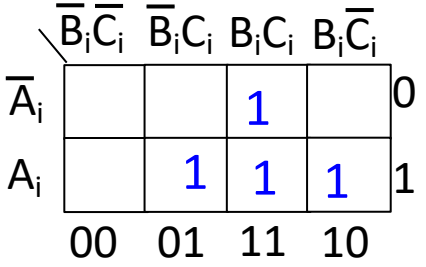
- Adds three 1-bit inputs
  - Inputs: A_i, B_i, C_i
  - Outputs: S_o, C_o
- Generate truth table
- Extract Boolean expressions
  - Using K-map

A_i	B_i	C_i	S_o	C_o
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

K-map for S_o



K-map for C_o



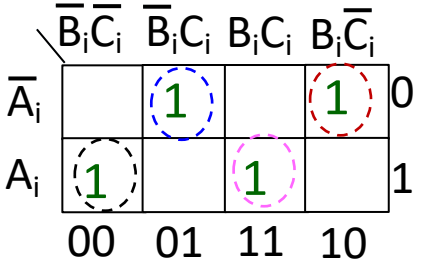
$S_o = \overline{A}_i\overline{B}_iC_i + \overline{A}_iB_i\overline{C}_i + A_i\overline{B}_i\overline{C}_i + A_iB_iC_i$

Simple adder design: full adder

- Adds three 1-bit inputs
  - Inputs: A_i, B_i, C_i
  - Outputs: S_o, C_o
- Generate truth table
- Extract Boolean expressions
  - Using K-map

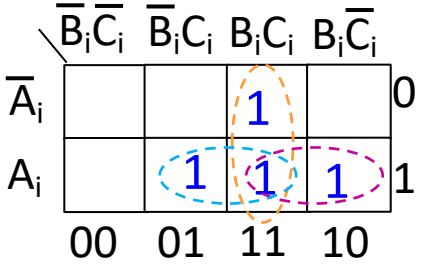
A_i	B_i	C_i	S_o	C_o
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

K-map for S_o



$S_o = \overline{A_i}\overline{B_i}C_i + \overline{A_i}B_i\overline{C_i} + A_i\overline{B_i}\overline{C_i} + A_iB_iC_i$

K-map for C_o



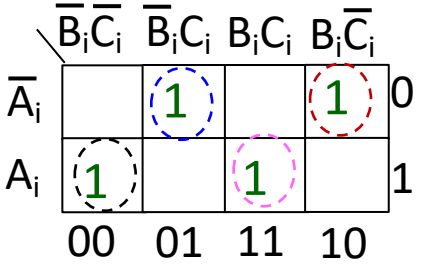
$C_o = A_iB_i + A_iC_i + B_iC_i$

Simple adder design: full adder

- Adds three 1-bit inputs
  - Inputs: A_i, B_i, C_i
  - Outputs: S_o, C_o
- Generate truth table
- Extract Boolean expressions
  - Using K-map
  - Simplify the expressions

A_i	B_i	C_i	S_o	C_o
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

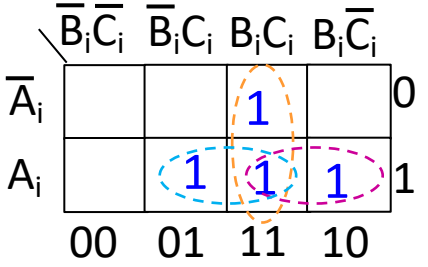
K-map for S_o



$S_o = \bar{A}_i\bar{B}_iC_i + \bar{A}_iB_i\bar{C}_i + A_i\bar{B}_i\bar{C}_i + A_iB_iC_i$

$S_o = A_i \oplus B_i \oplus C_i$

K-map for C_o



$C_o = A_iB_i + A_iC_i + B_iC_i$

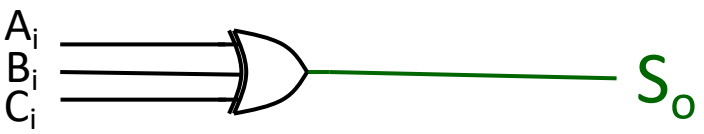
Full adder circuit implementation

- Combinational implementation

Full adder circuit implementation

- Combinational implementation

  $S_o = A_i \oplus B_i \oplus C_i$

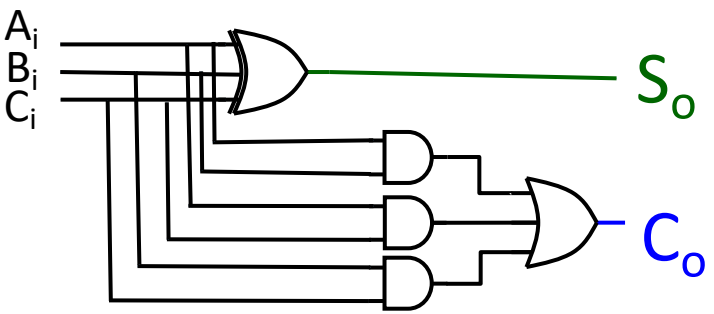


Full adder circuit implementation

- Combinational implementation

  $S_o = A_i \oplus B_i \oplus C_i$

  $C_o = A_iB_i + A_iC_i + B_iC_i$

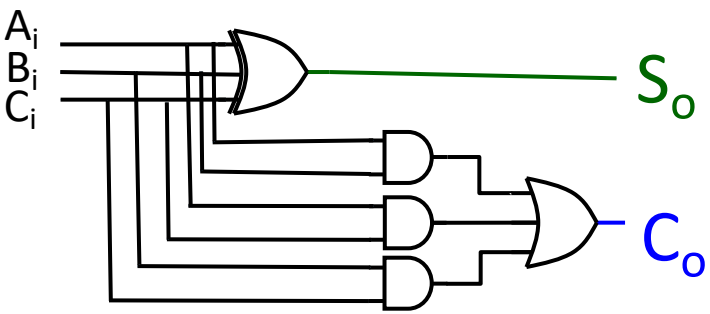


Full adder circuit implementation

- Combinational implementation

  $S_o = A_i \oplus B_i \oplus C_i$

  $C_o = A_iB_i + A_iC_i + B_iC_i$



Is there any drawback?

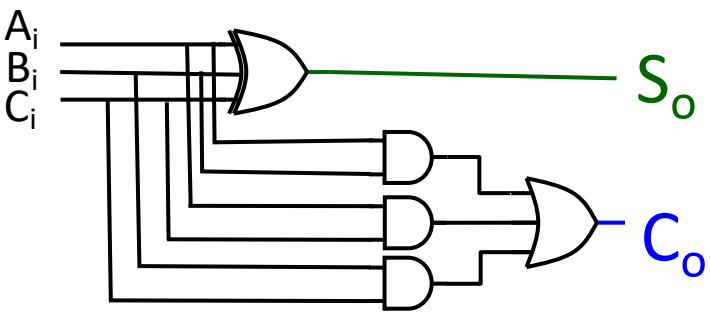
Full adder circuit implementation

- Combinational implementation

  $S_o = A_i \oplus B_i \oplus C_i$

  $C_o = A_iB_i + A_iC_i + B_iC_i$

- Using two half adders



Is there any drawback?

Full adder circuit implementation

- Combinational implementation

  $S_o = A_i \oplus B_i \oplus C_i$

  $C_o = A_iB_i + A_iC_i + B_iC_i$

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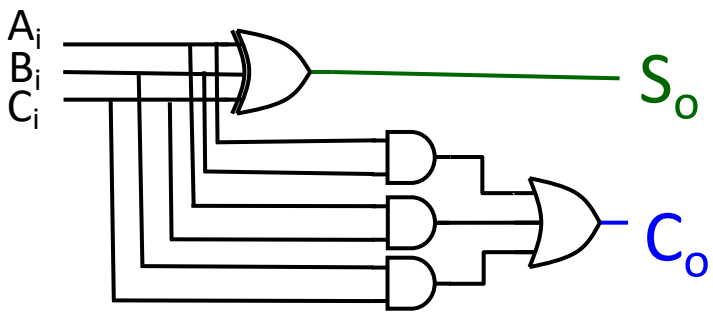

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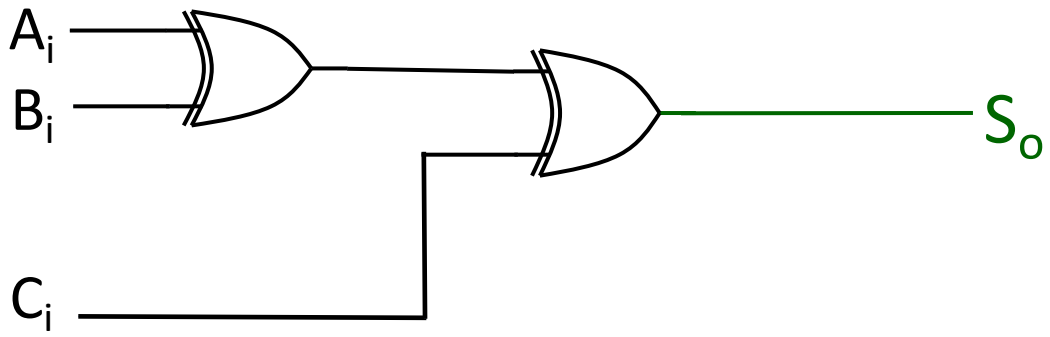

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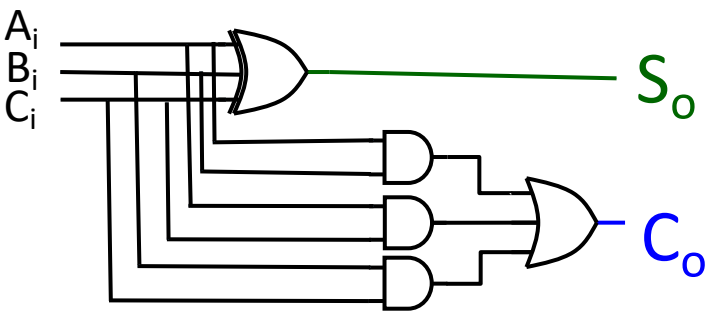

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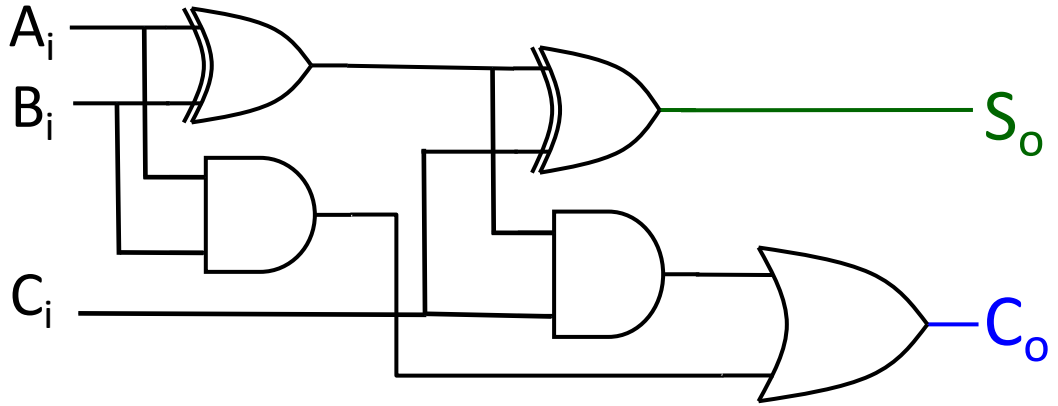

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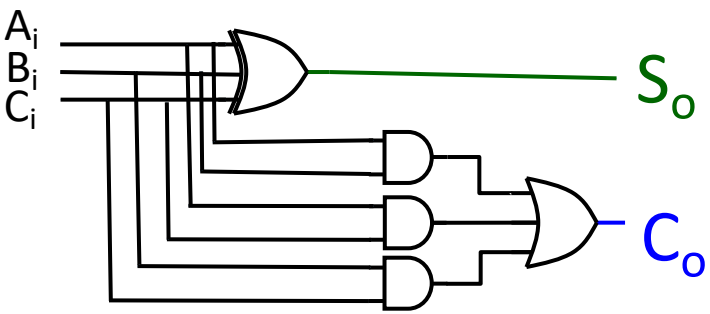

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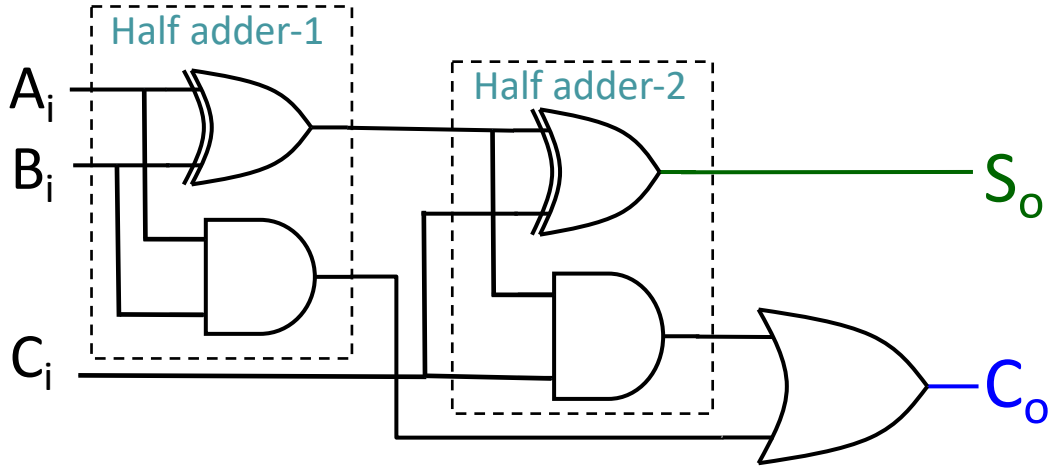

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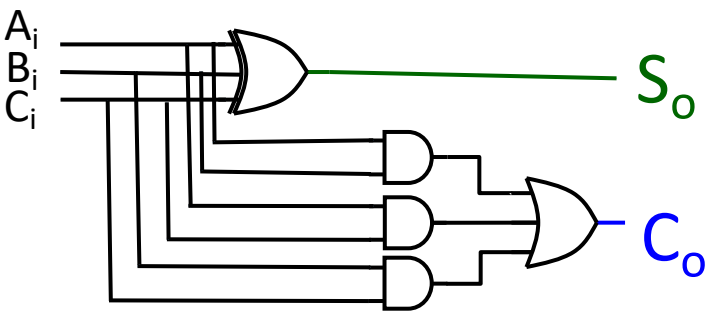

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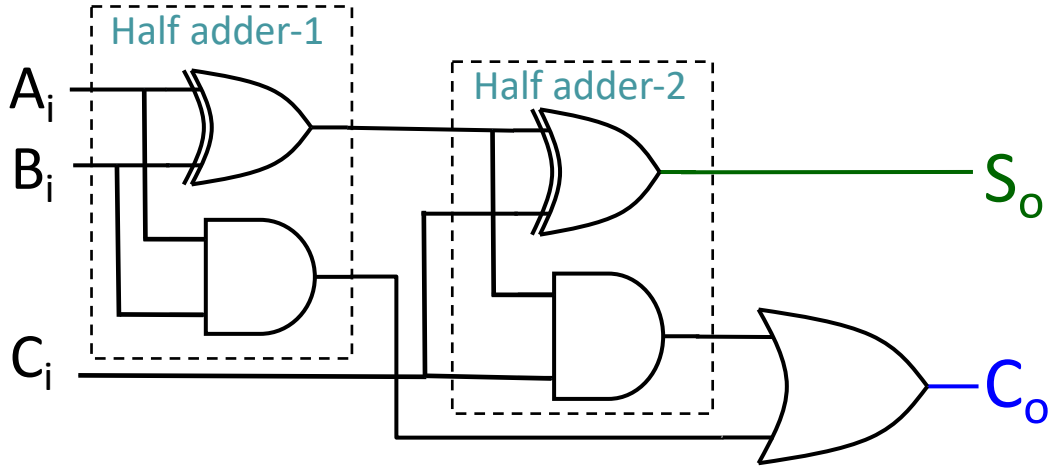

- Full Adder (FA) block diagram

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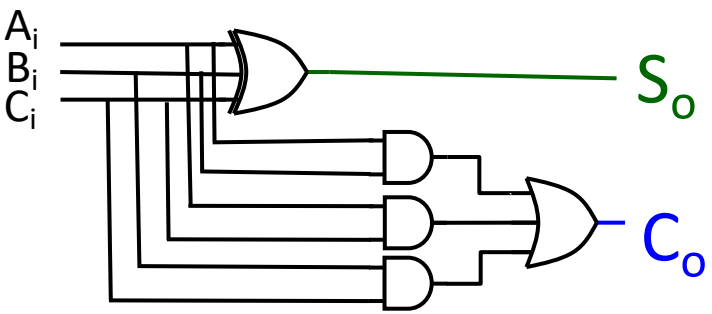

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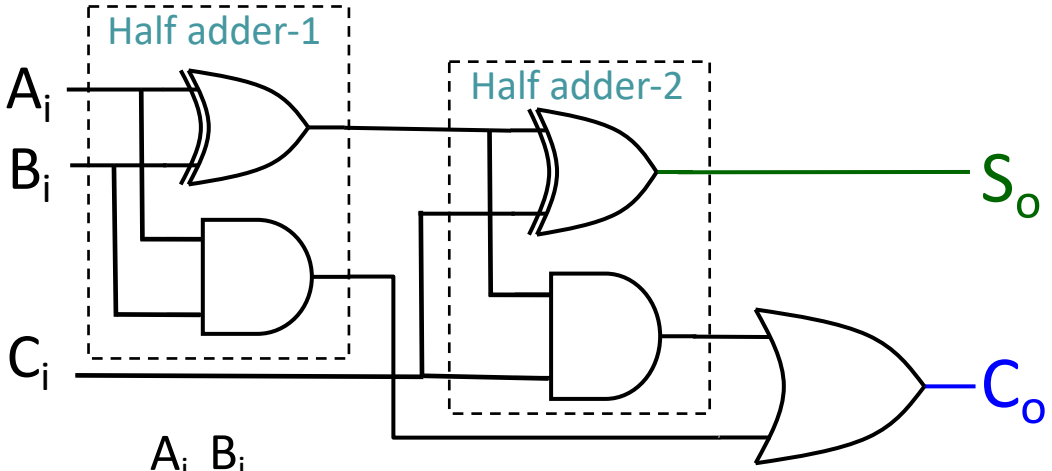

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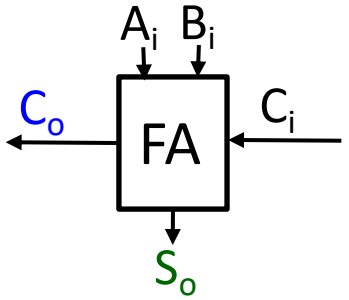
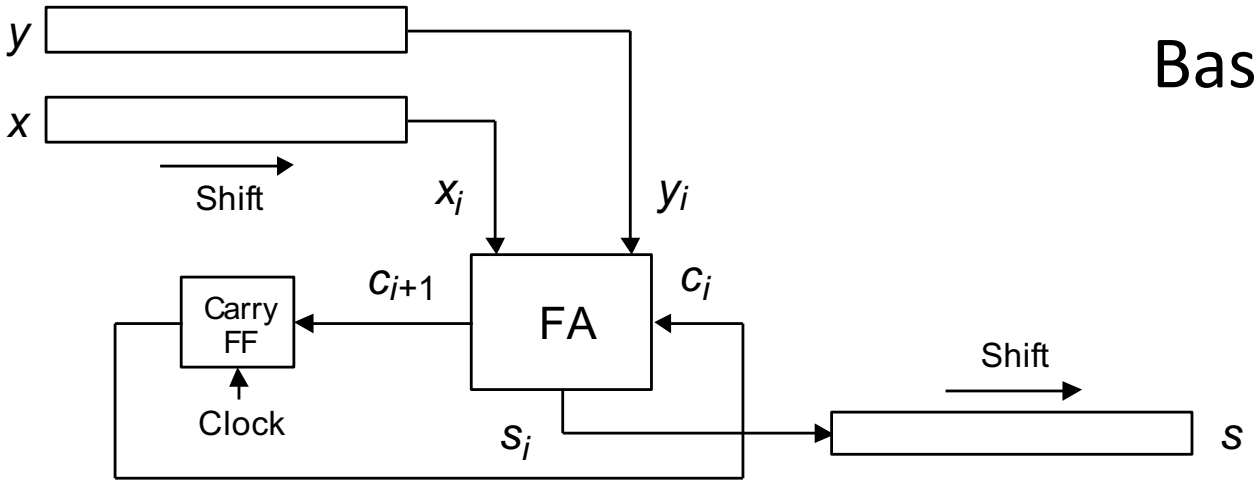


Building simple adders using full adder



(a) Bit-serial adder.

Basics of bit-serial adder

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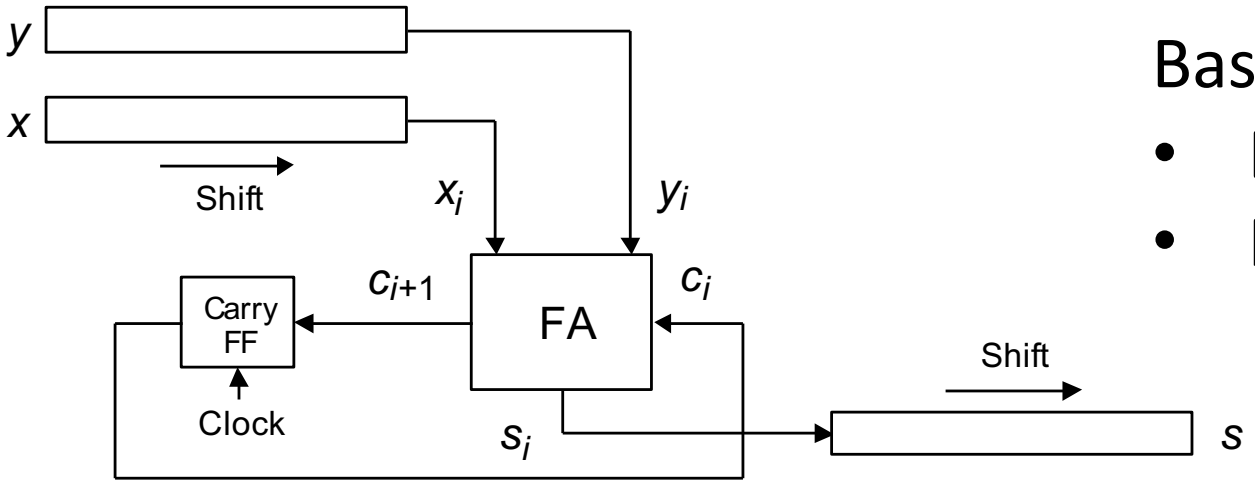

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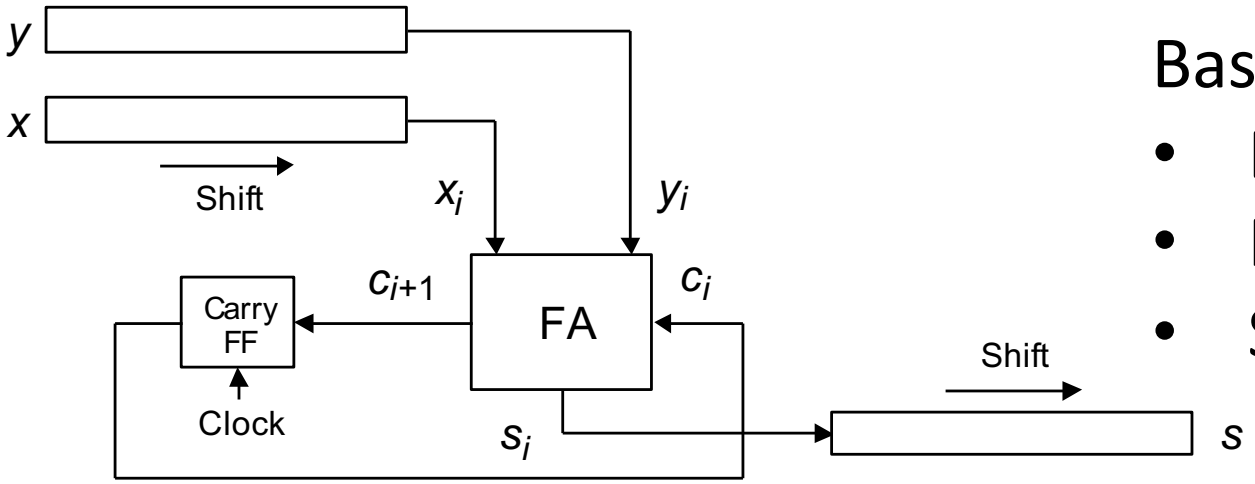

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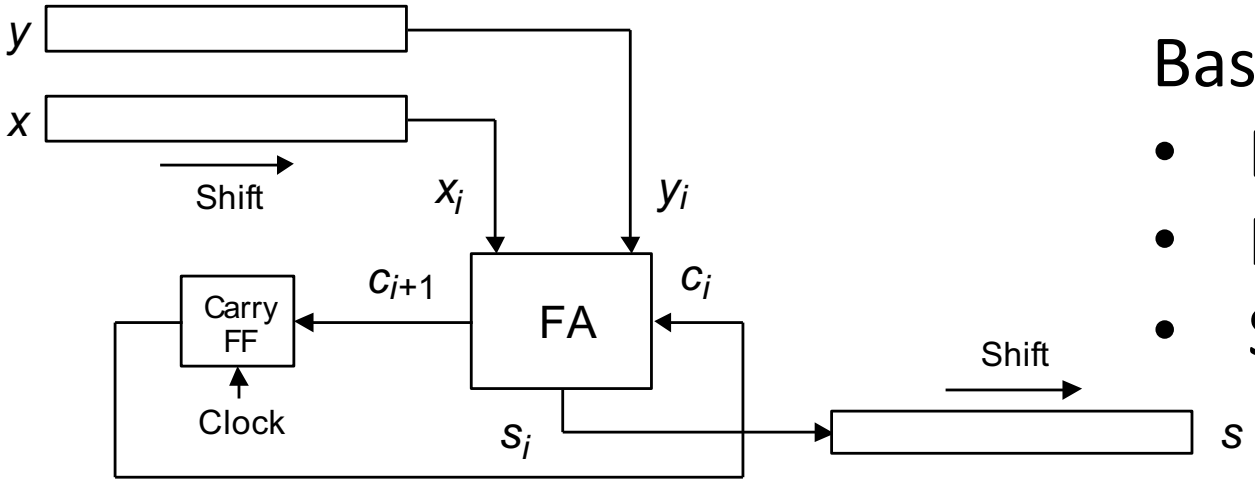

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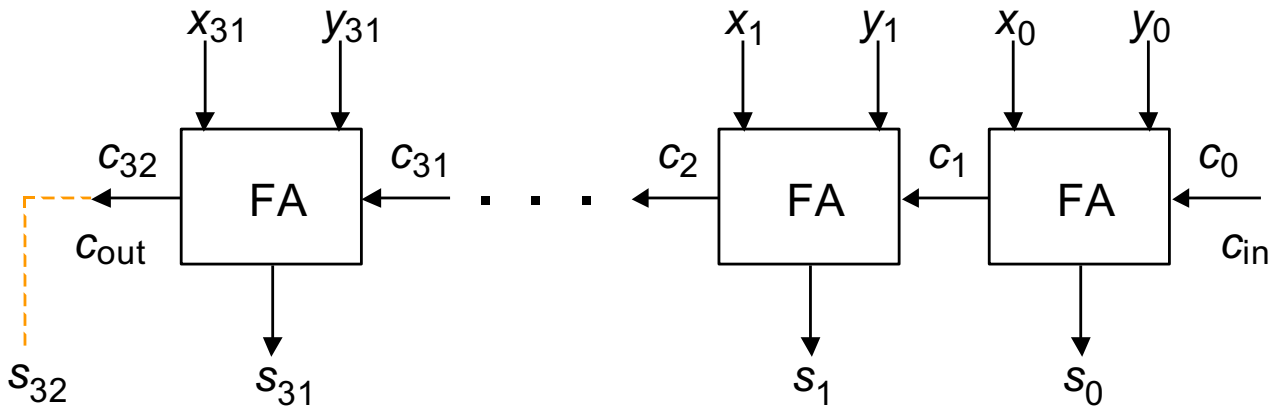

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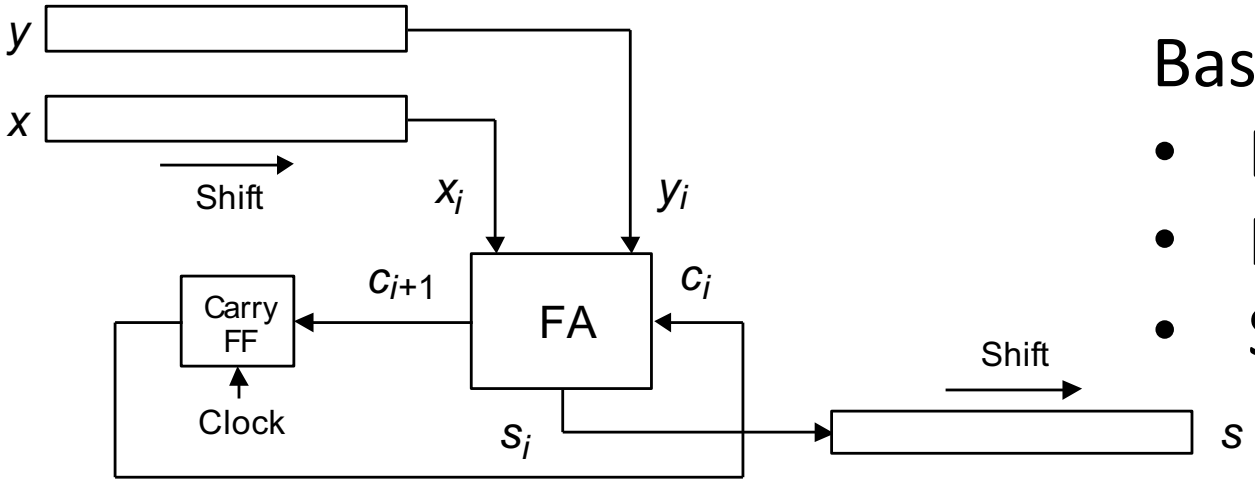

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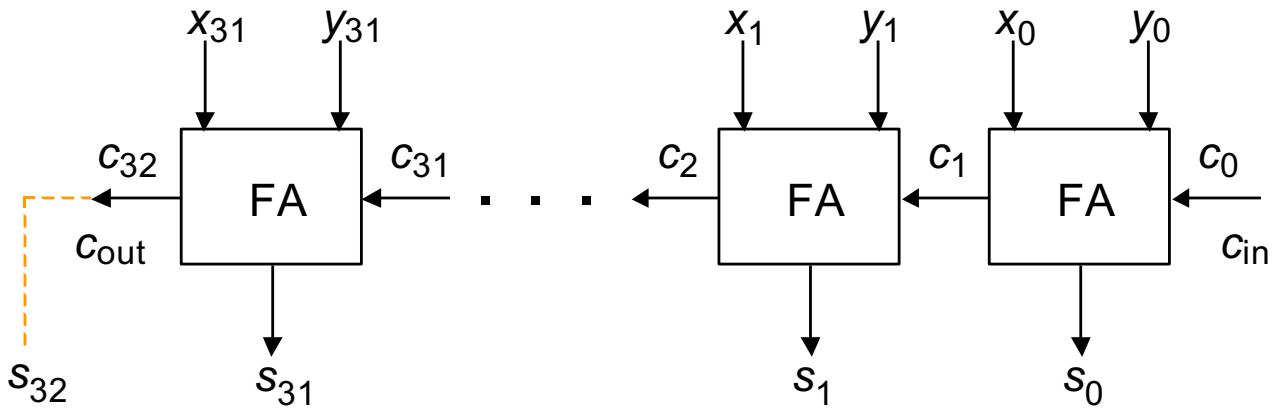

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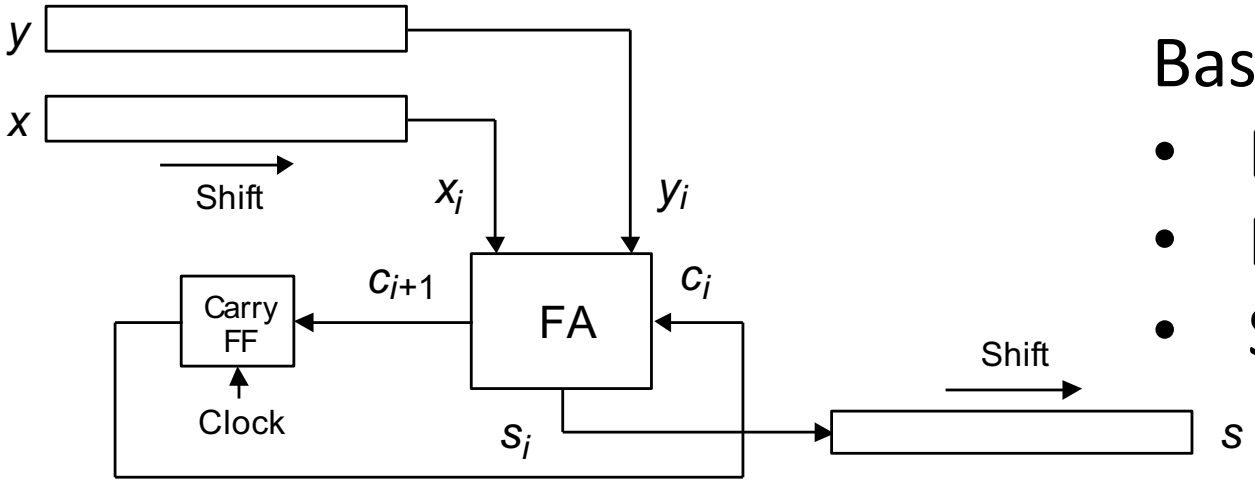

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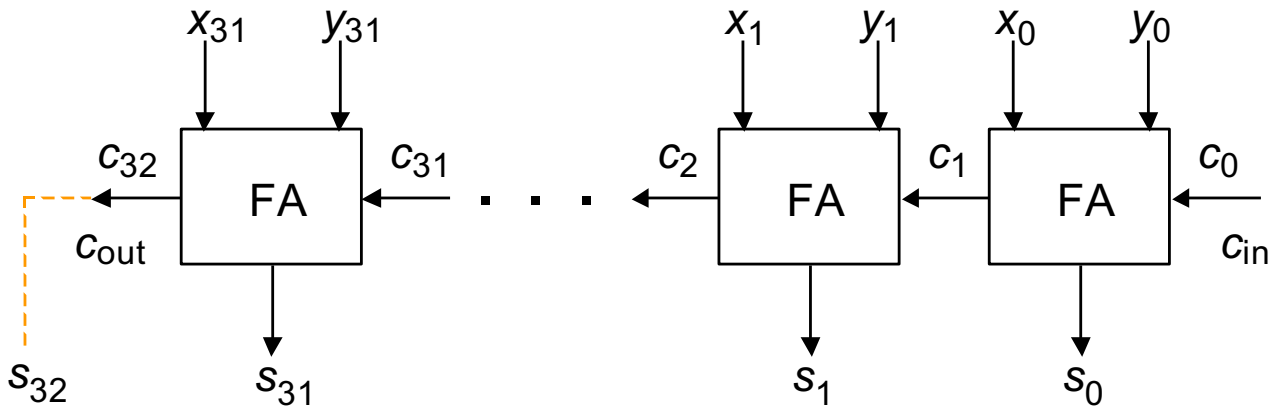

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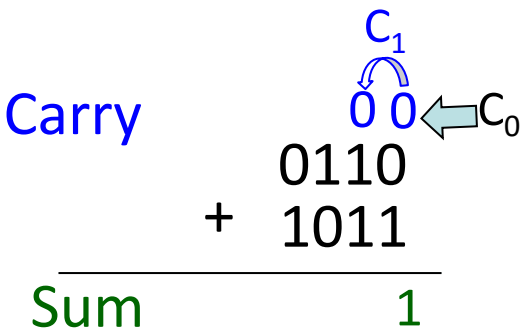

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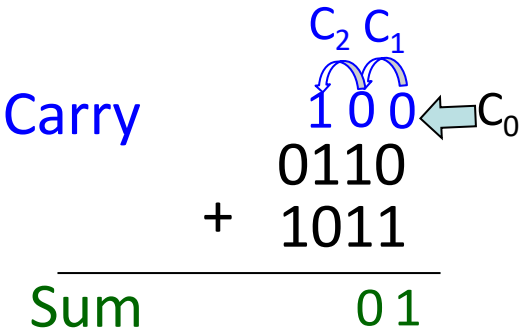

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		0	1	1	0
	+	1	0	1	1
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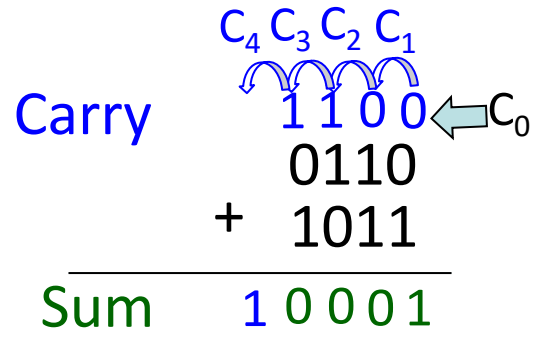

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Carry $C_4\ C_3\ C_2\ C_1$: 1 1 0 0 ⇦ C_0

0110

\+ 1011

Sum 1 0 0 0 1

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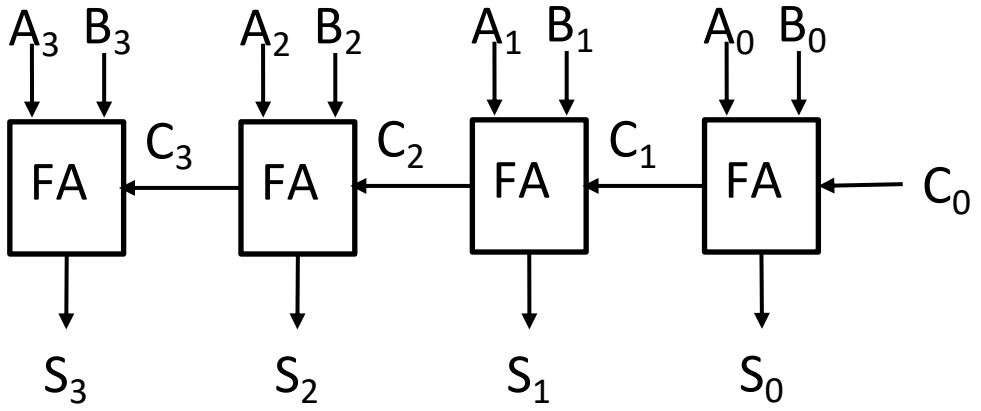

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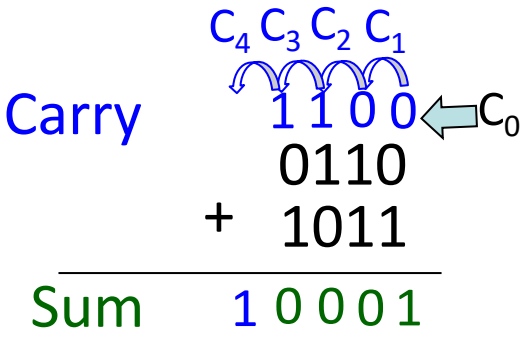

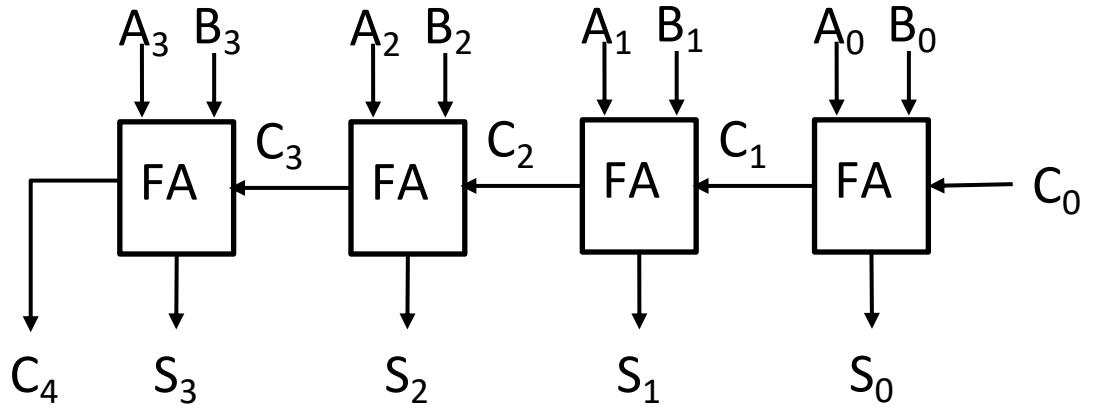

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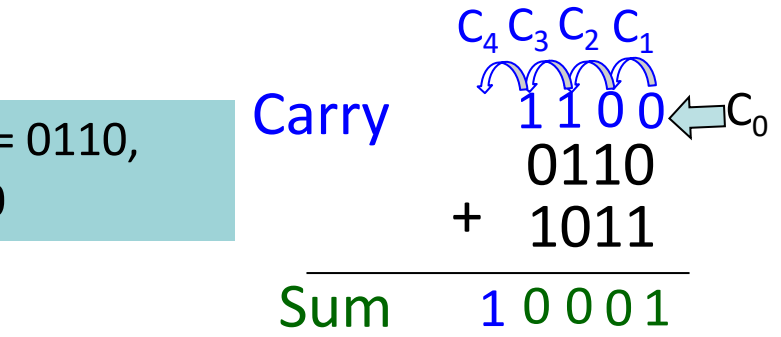

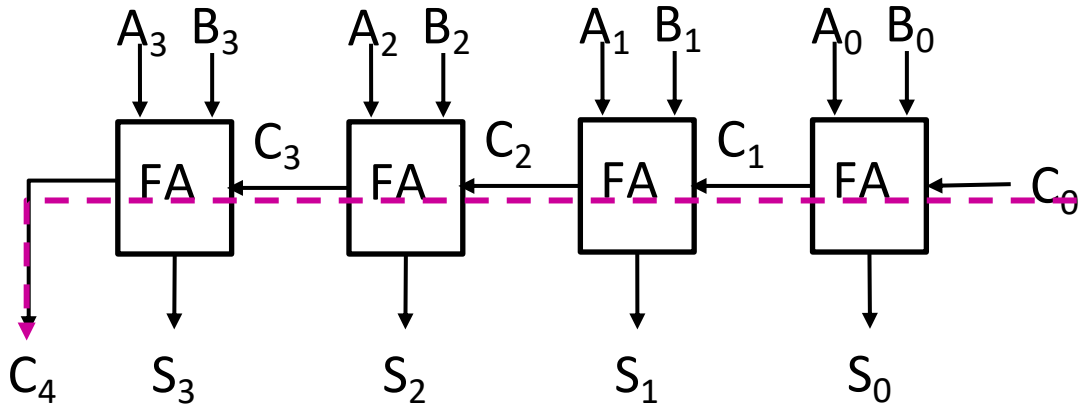

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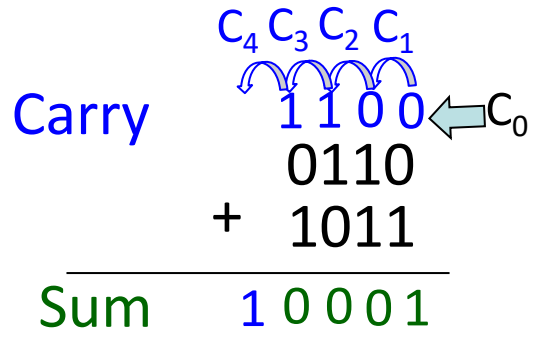

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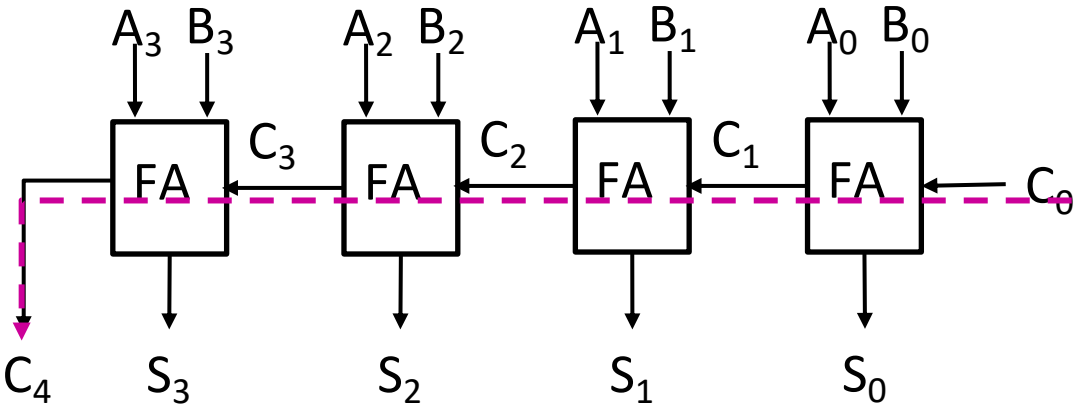

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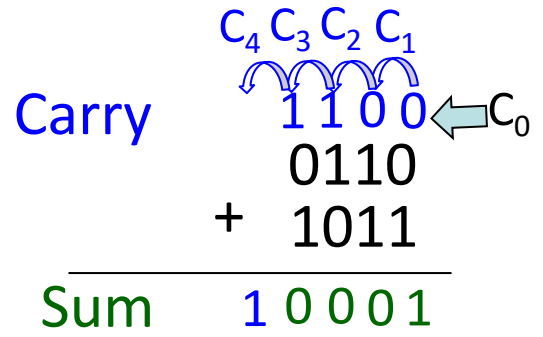
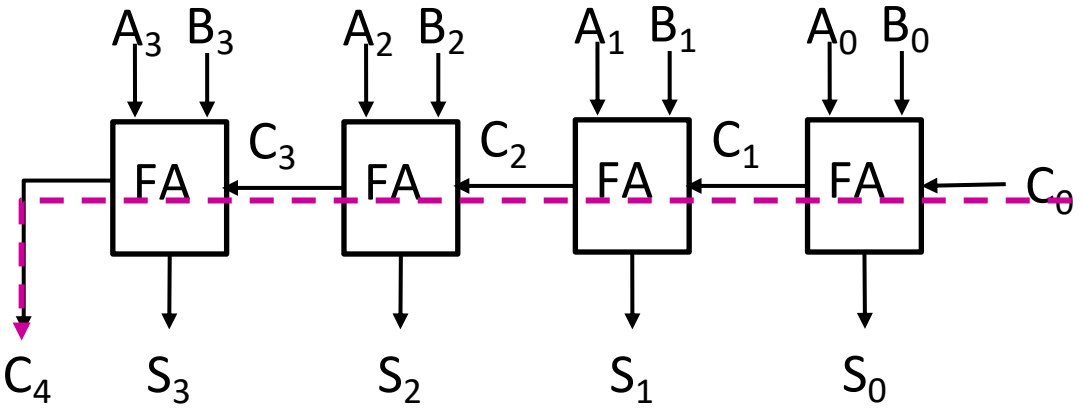
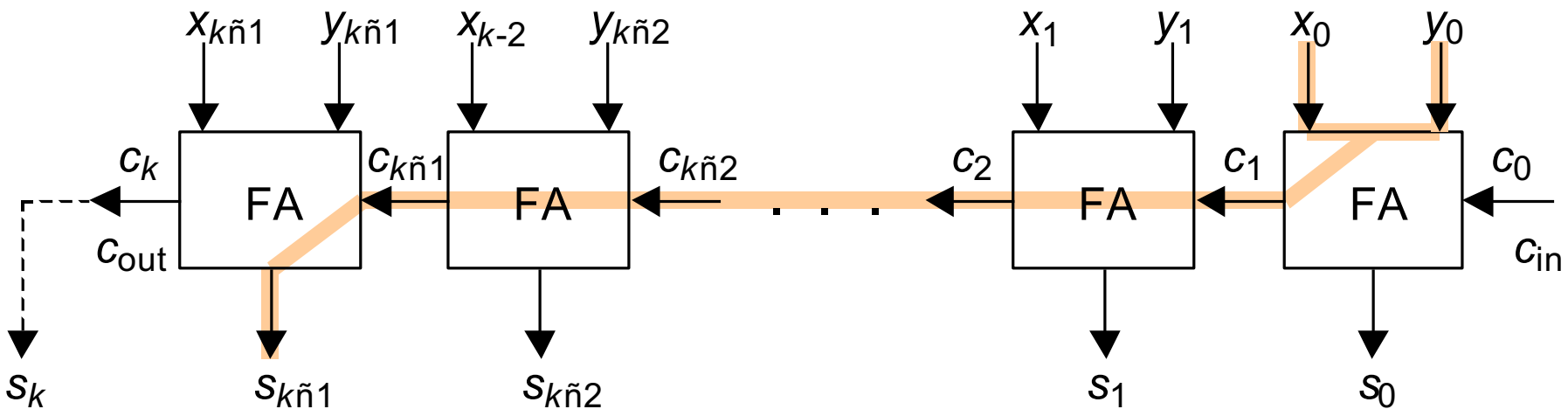




Can we do it faster?

Carry path of ripple-carry adder

$$T_{\text{ripple-add}} = T_{FA}(x,y \rightarrow c_{out}) + (k-2) \times T_{FA}(c_{in} \rightarrow cout) + T_{FA}(c_{in} \rightarrow s)$$



Critical path in a *k*-bit ripple-carry adder.

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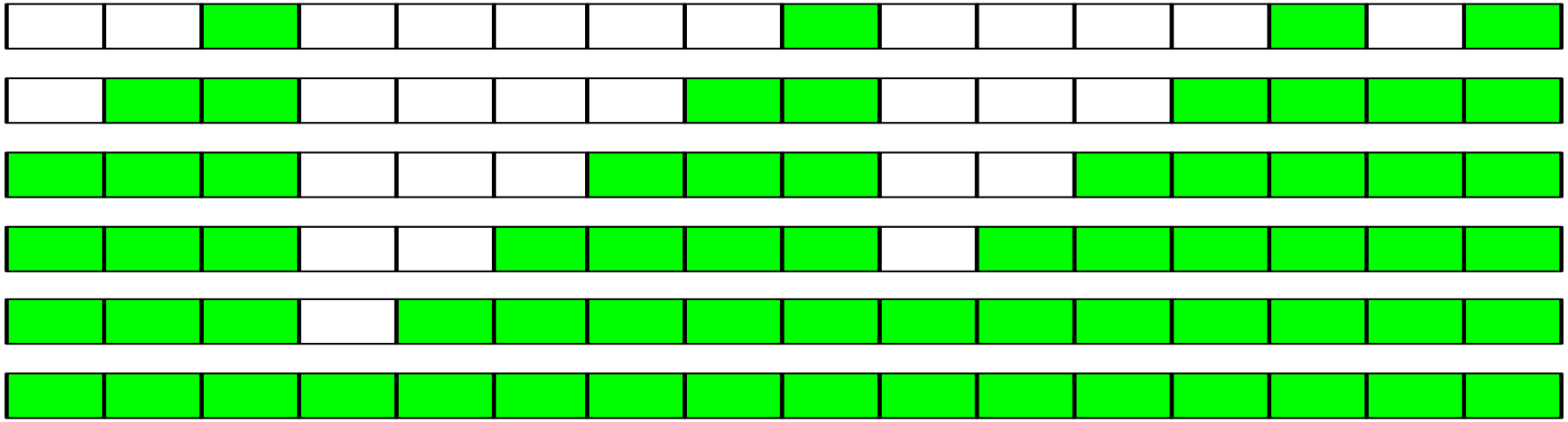
Critical path and carry propagation example in a *16*-bit ripple-carry addition



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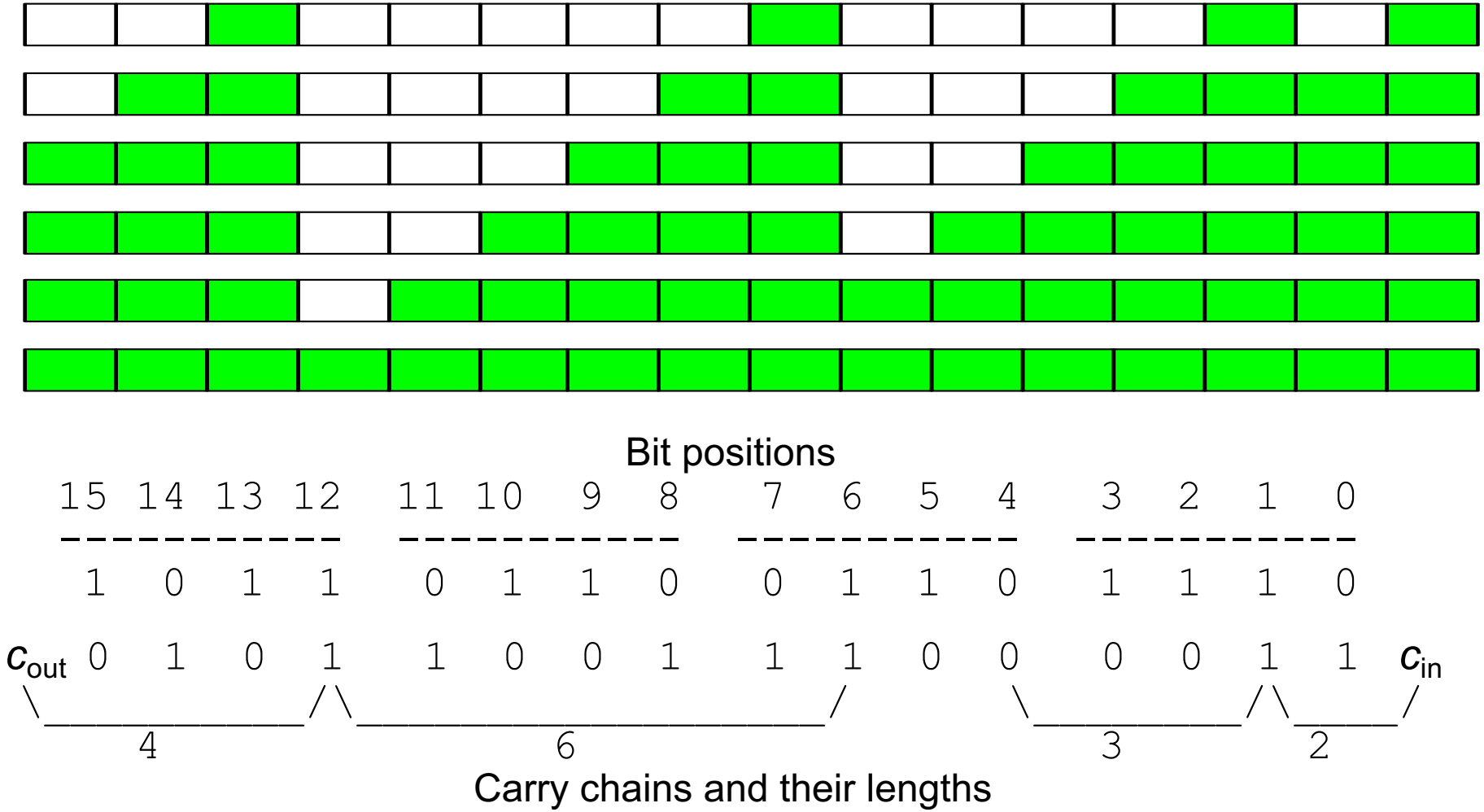

Carry propagation analysis

Given binary numbers with random bits, for each position *i* we have

- Average length of the longest carry chain in *k*-bit addition is strictly less than $\log_2 k$; it is $\log_2(1.25k)$ per experimental results

Analogy: Expected number when rolling one die is 3.5; if one rolls many dice, the expected value of the largest number shown grows

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  $2 - 2^{-(k-i-1)}$

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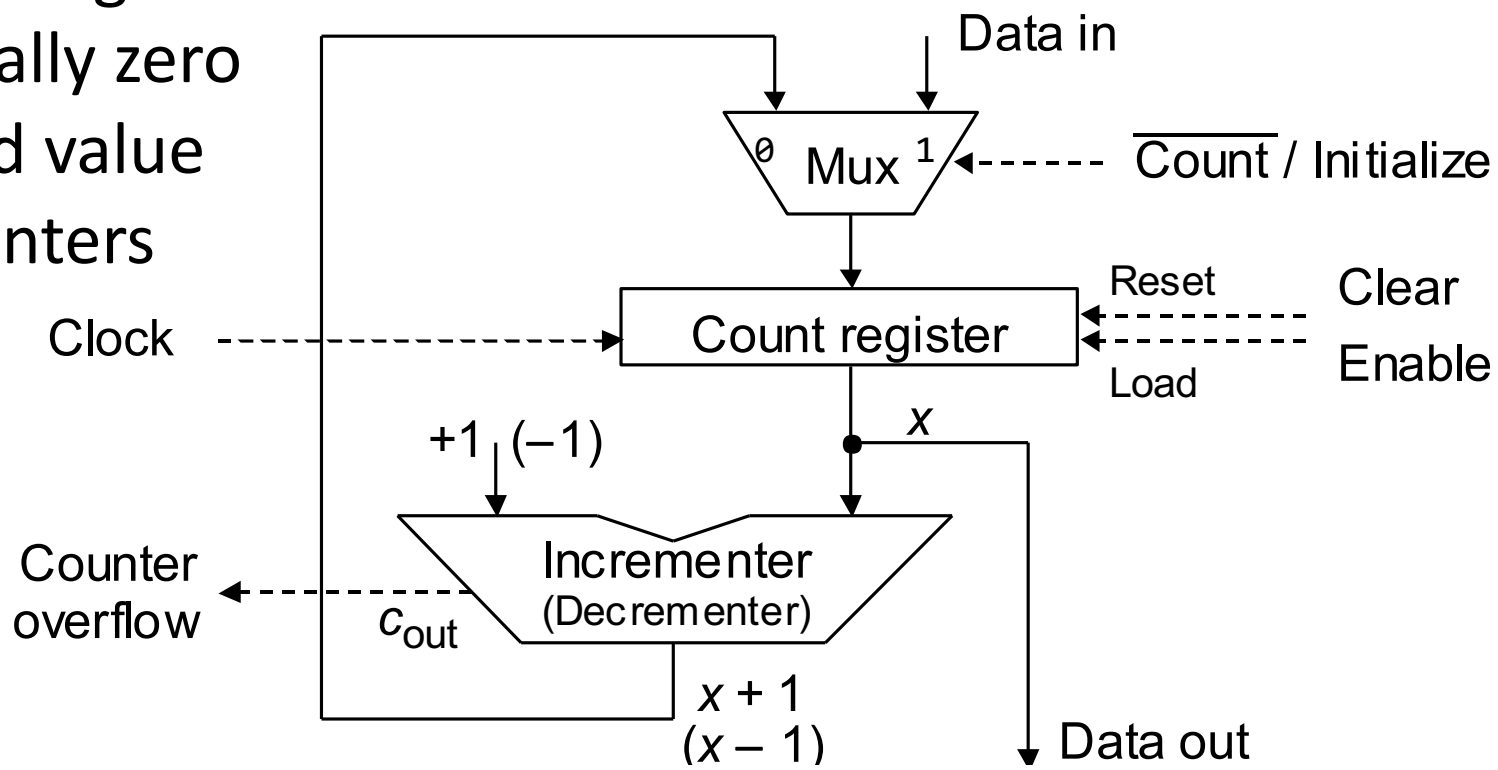
An up (down) counter built of a register, an adder and a multiplexer.



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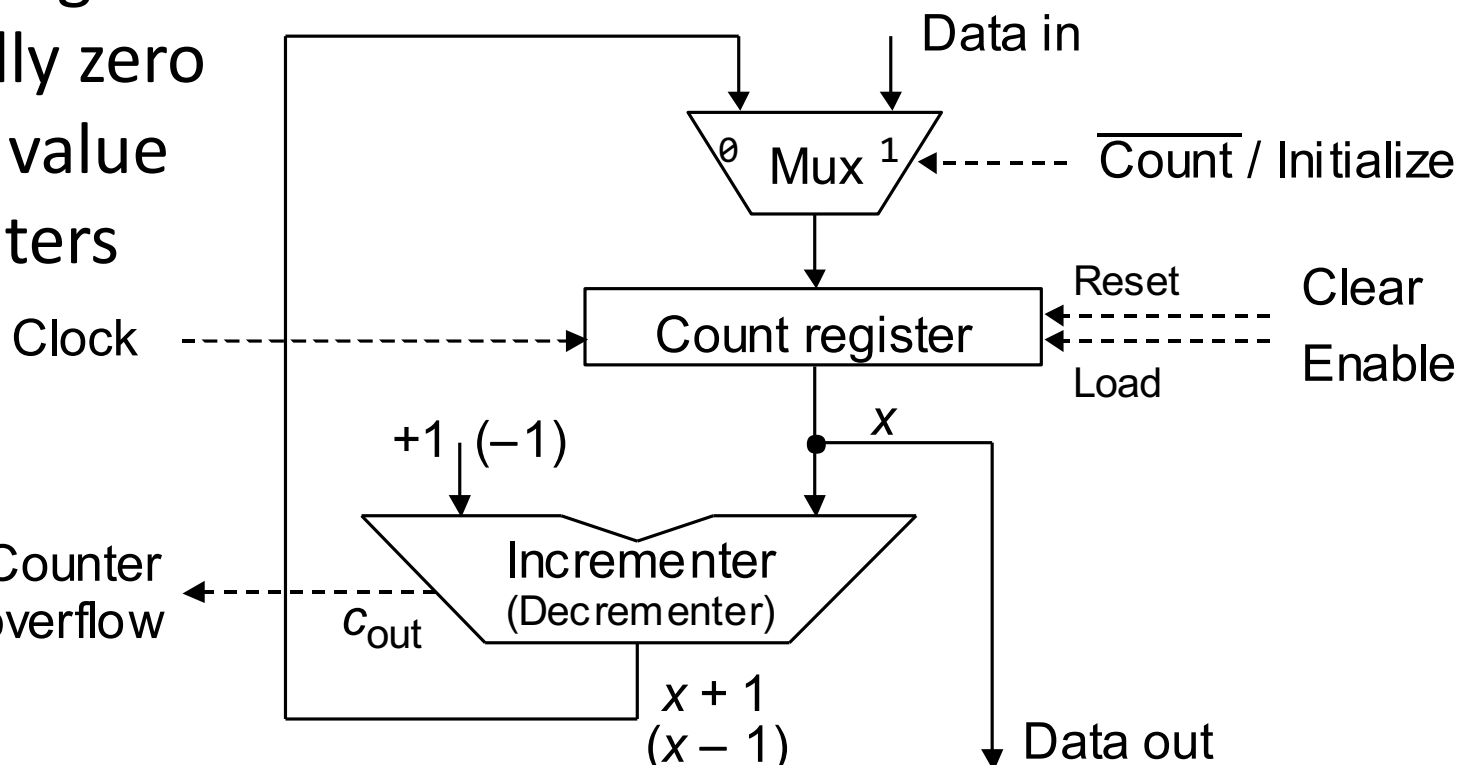
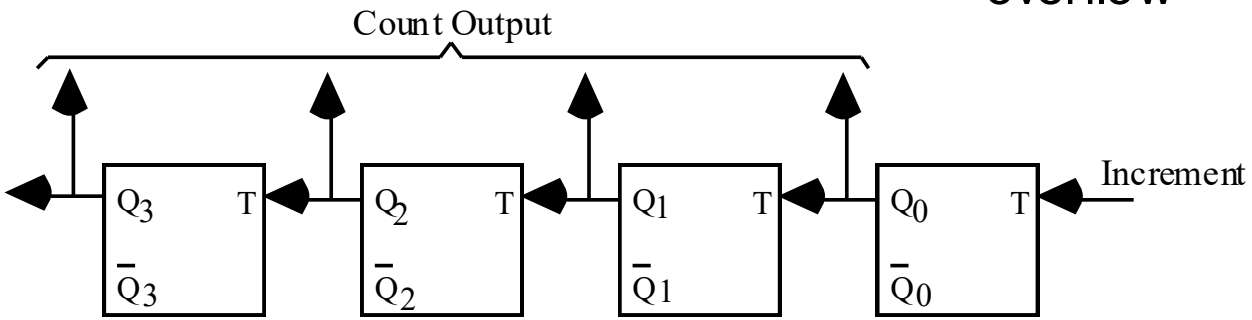
An up (down) counter built of a register, an adder and a multiplexer.



Four-bit asynchronous up counter built using T flip-flops



Fast Addition

Carry network is the essence of fast adders

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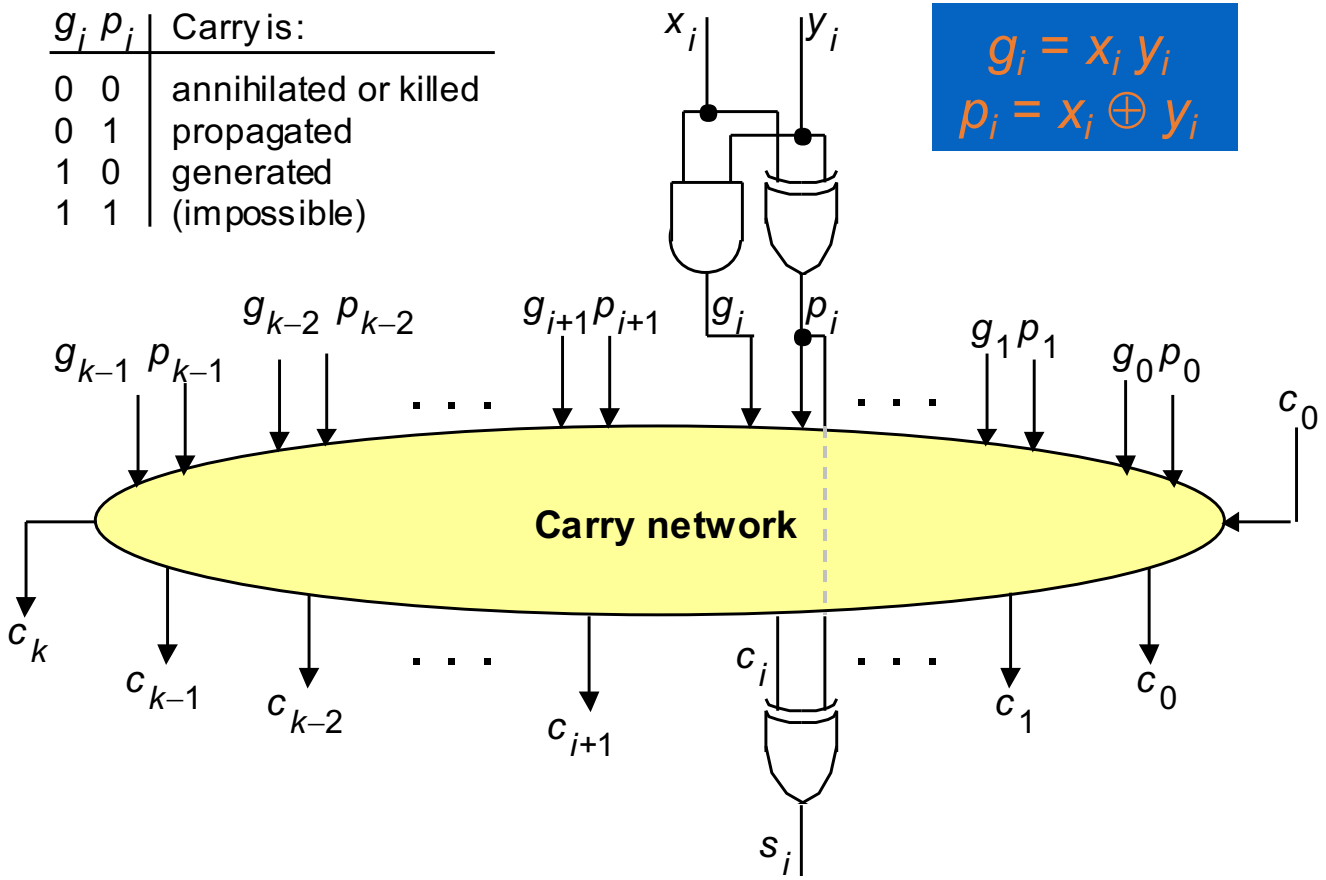
g_i	p_i	Carry is:
0	0	annihilated or killed
0	1	propagated
1	0	generated
1	1	(impossible)

$g_i = x_i\, y_i$

$p_i = x_i \oplus y_i$



Generic structure of a binary adder, highlighting its carry network.

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Carry network is the essence of fast adders

Ripple-Carry Adder Revisited

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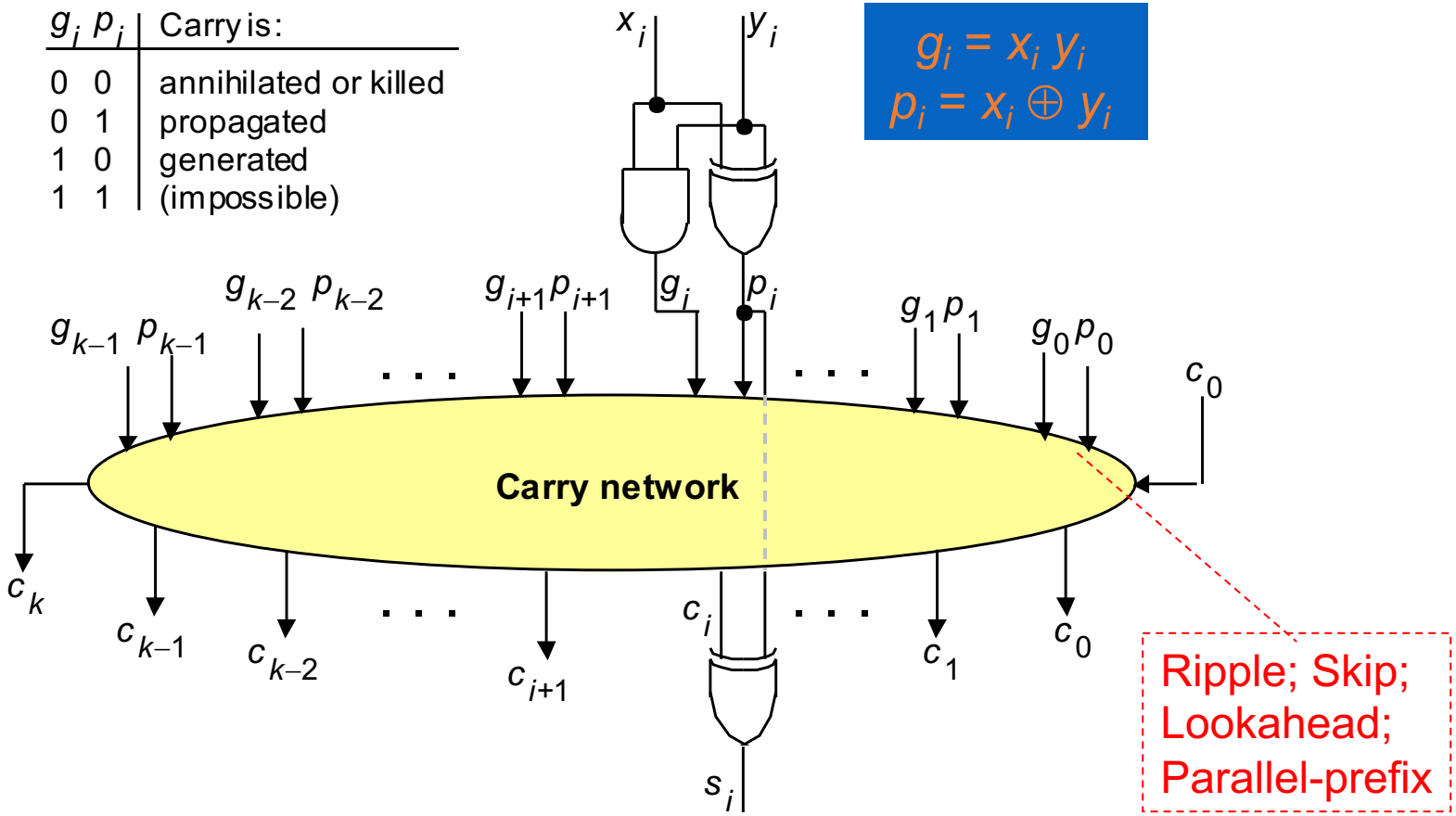

Ripple; Skip;
Lookahead;
Parallel-prefix

Generic structure of a binary adder, highlighting its carry network.

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The carry recurrence: $c_{i+1} = g_i \vee p_i\, c_i$

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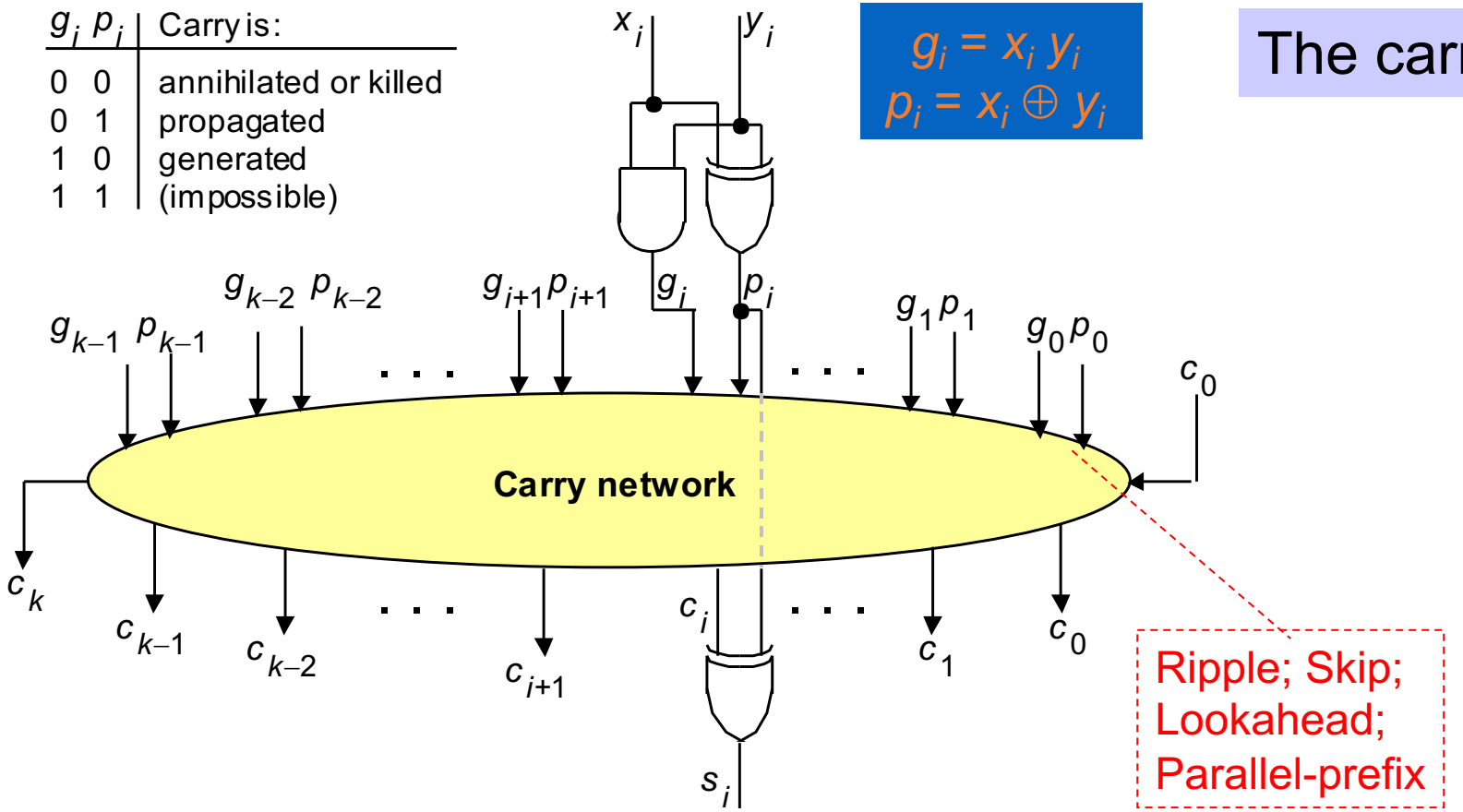

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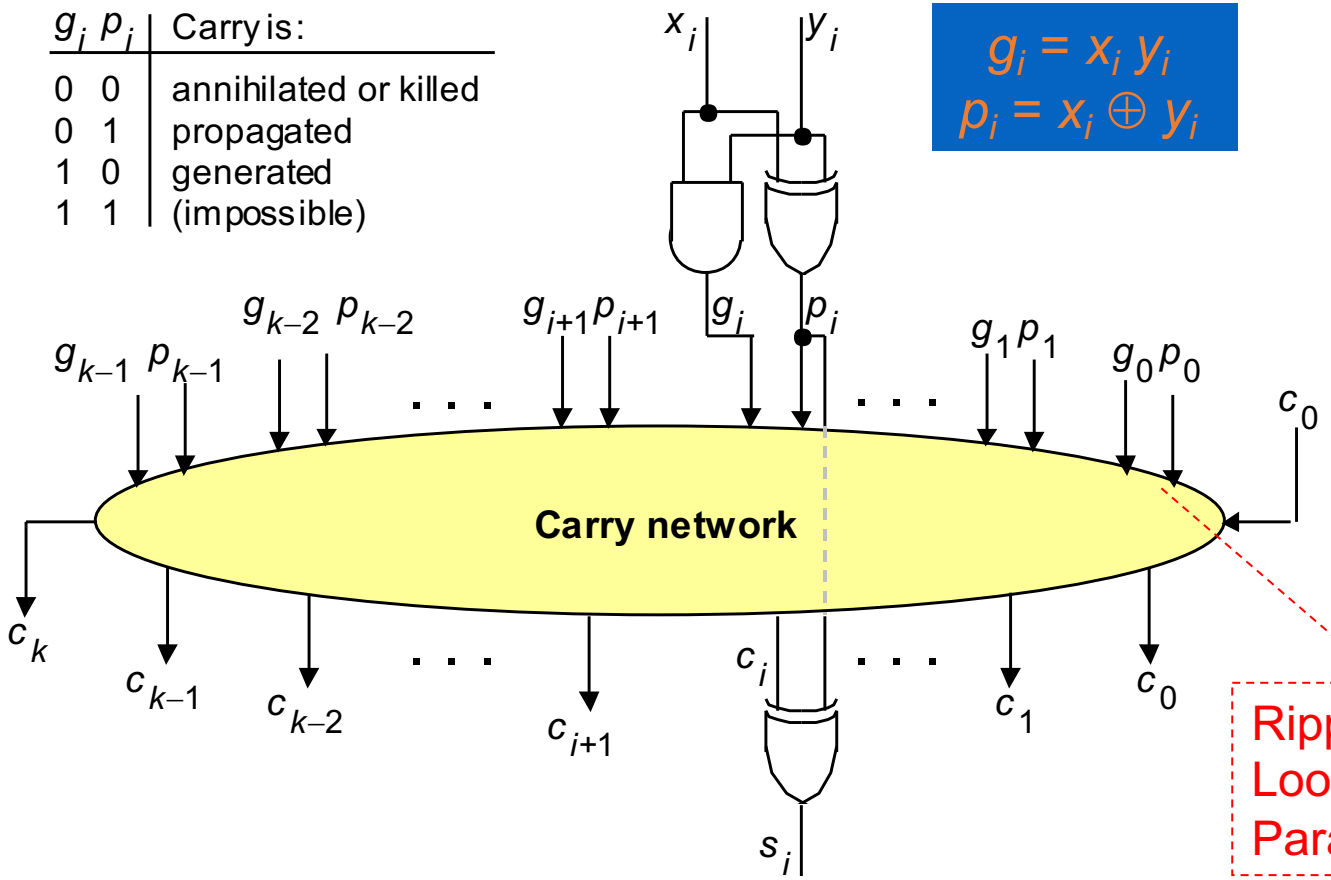

Ripple-Carry Adder Revisited

The carry recurrence: $c_{i+1} = g_i \vee p_i\, c_i$

Latency of k-bit adder is roughly $2k$ gate delays:

- 1 gate delay for production of p and g signals, plus
- $2(k-1)$ gate delays for carry propagation, plus
- 1 XOR gate delay for generation of the sum bits

Ripple; Skip; Lookahead; Parallel-prefix

Generic structure of a binary adder, highlighting its carry network.

Carry-Lookahead Adders

Recall the *generate*, *propagate*, *annihilate* (*absorb*), and *transfer* signals:

Carry-Lookahead Adders

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Signal	Radix r	Binary
g_i	is 1 iff $x_i + y_i \geq r$	$x_i\, y_i$
p_i	is 1 iff $x_i + y_i = r - 1$	$x_i \oplus y_i$
a_i	is 1 iff $x_i + y_i < r - 1$	$x_i' y_i' = (x_i \vee y_i)'$
t_i	is 1 iff $x_i + y_i \geq r - 1$	$x_i \vee y_i$
s_i	$(x_i + y_i + c_i) \bmod r$	$x_i \oplus y_i \oplus c_i$

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The carry recurrence can be unrolled to obtain each carry signal directly from inputs, rather than through propagation

$$
\begin{aligned}
c_i &= g_{i-1} \vee c_{i-1} p_{i-1} \\
&= g_{i-1} \vee (g_{i-2} \vee c_{i-2} p_{i-2}) p_{i-1} \\
&= g_{i-1} \vee g_{i-2} p_{i-1} \vee c_{i-2} p_{i-2} p_{i-1} \\
&= g_{i-1} \vee g_{i-2} p_{i-1} \vee g_{i-3} p_{i-2} p_{i-1} \vee c_{i-3} p_{i-3} p_{i-2} p_{i-1} \\
&= g_{i-1} \vee g_{i-2} p_{i-1} \vee g_{i-3} p_{i-2} p_{i-1} \vee g_{i-4} p_{i-3} p_{i-2} p_{i-1} \vee c_{i-4} p_{i-4} p_{i-3} p_{i-2} p_{i-1} \\
&= \ldots
\end{aligned}
$$

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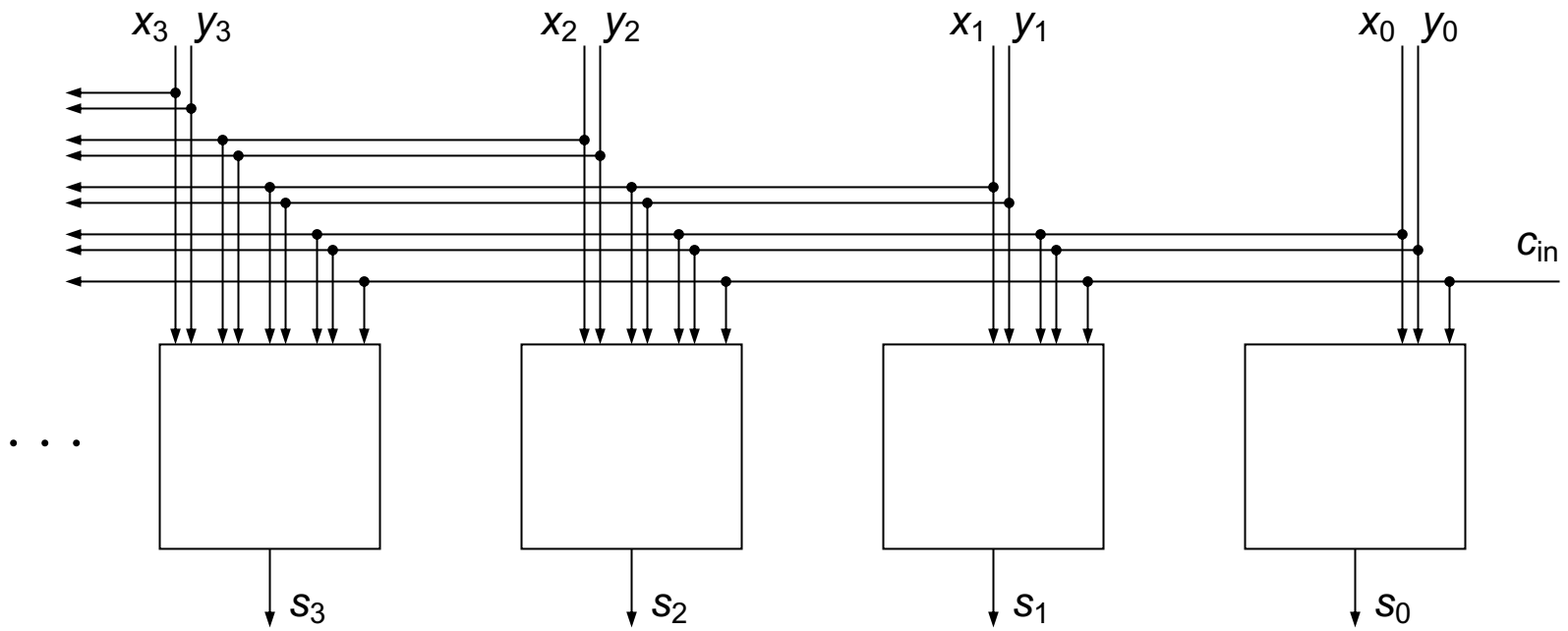
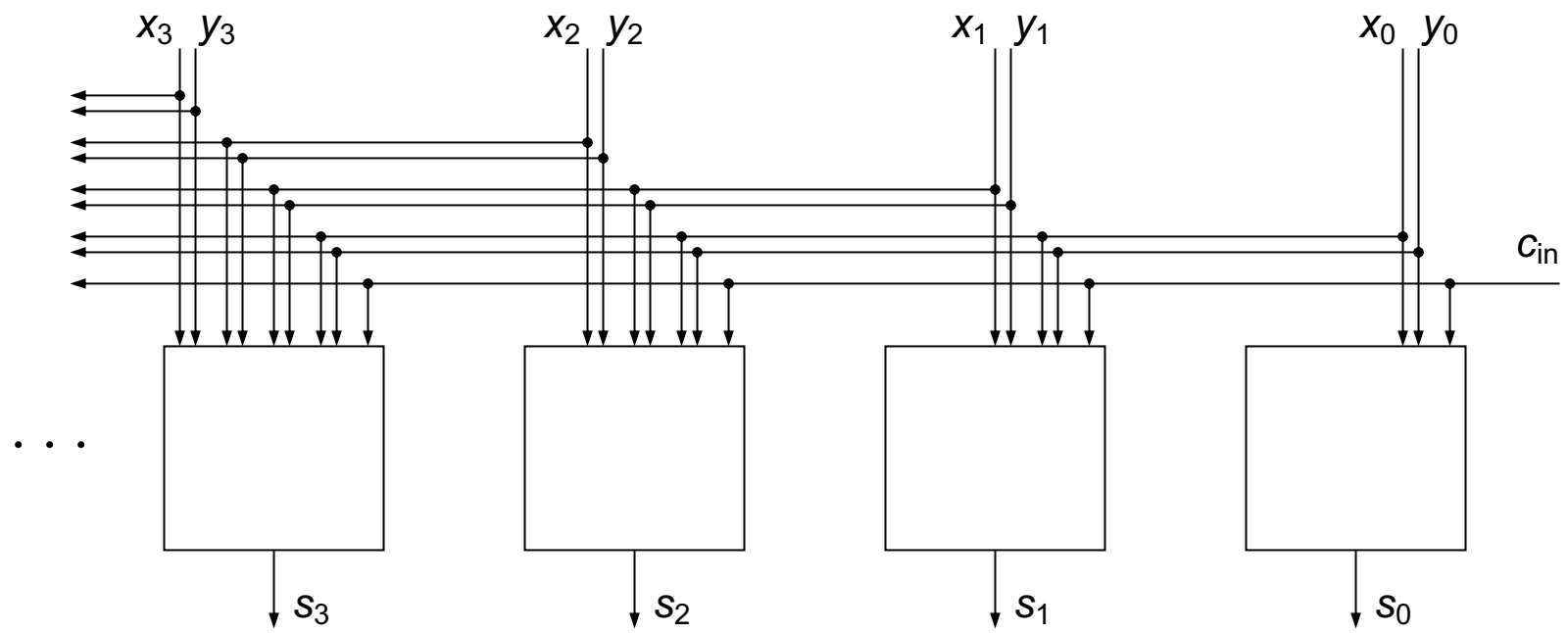
&= \ldots
\end{aligned}
$$

Note:
Addition symbol vs logical OR

Carry-lookahead adders



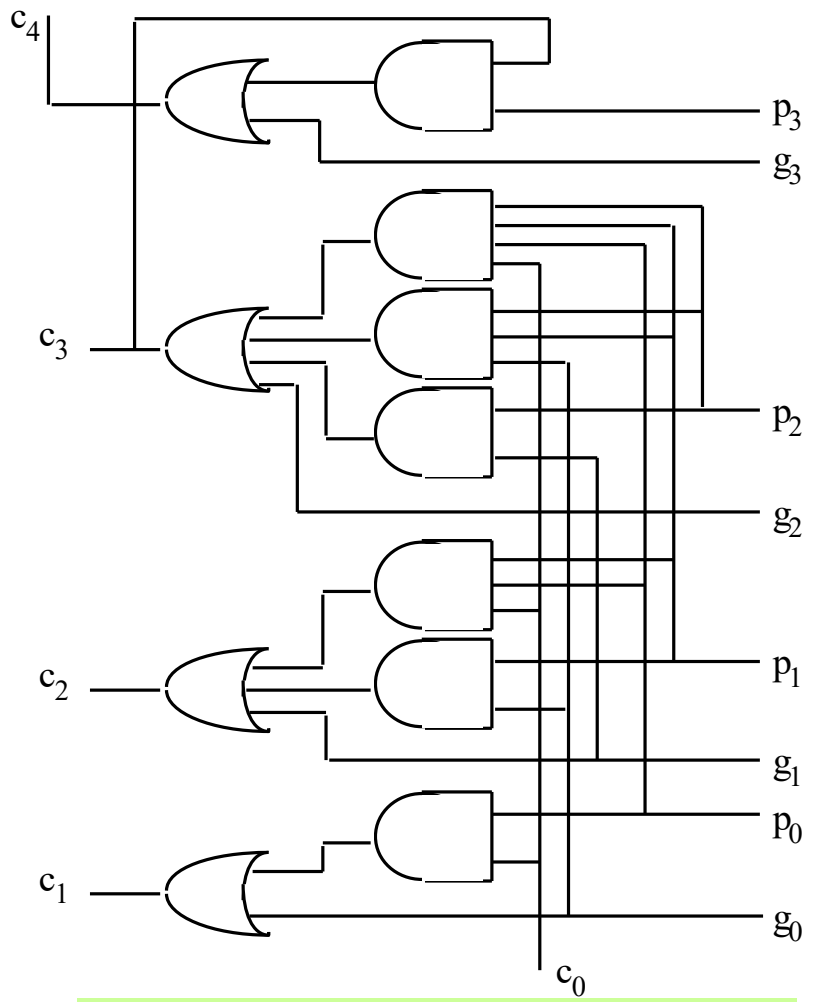
Carry-lookahead adders



Theoretically, it is possible to derive each sum digit directly from the inputs that affect it

Carry-lookahead adder design is simply a way of reducing the complexity of this ideal, but impractical, arrangement by hardware sharing among the various lookahead circuits

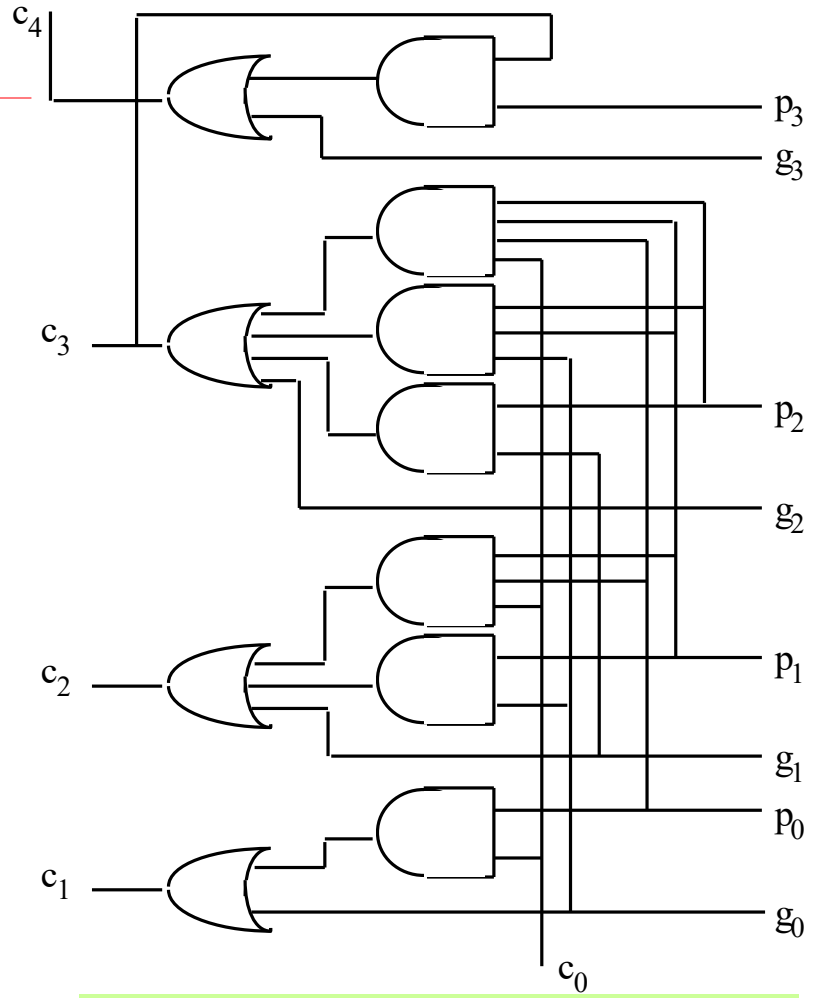
Carry-lookahead adders: 4-bit example



Four-bit carry network with full lookahead

Carry-lookahead adders: 4-bit example

Complexity reduced by deriving the carry-out indirectly



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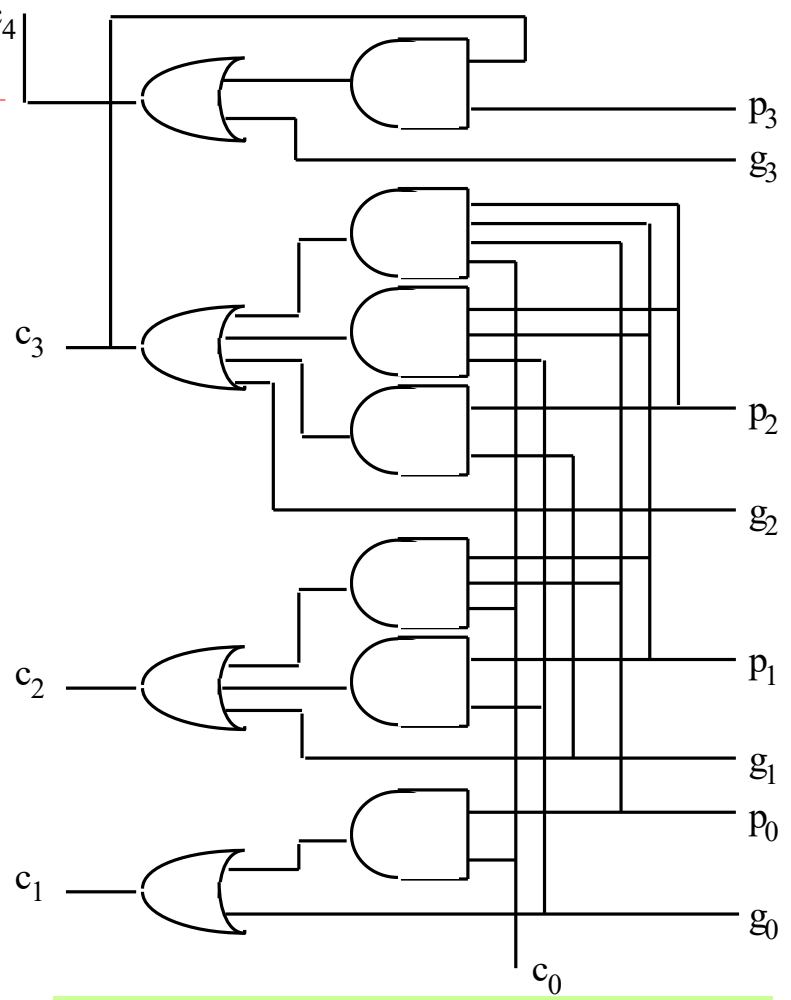

Four-bit carry network with full lookahead

Full carry lookahead is quite practical for a 4-bit adder

$$c_1 = g_0 \vee c_0 p_0$$
$$c_2 = g_1 \vee g_0 p_1 \vee c_0 p_0 p_1$$
$$c_3 = g_2 \vee g_1 p_2 \vee g_0 p_1 p_2 \vee c_0 p_0 p_1 p_2$$
$$c_4 = g_3 \vee g_2 p_3 \vee g_1 p_2 p_3 \vee g_0 p_1 p_2 p_3 \vee c_0 p_0 p_1 p_2 p_3$$

Carry-lookahead adders: beyond 4-bits

Consider a 32-bit adder

$c_1 = g_0 \vee c_0 p_0$

$c_2 = g_1 \vee g_0 p_1 \vee c_0 p_0 p_1$

$c_3 = g_2 \vee g_1 p_2 \vee g_0 p_1 p_2 \vee c_0 p_0 p_1 p_2$

.

.

.

$c_{31} = g_{30} \vee g_{29} p_{30} \vee g_{28} p_{29} p_{30} \vee g_{27} p_{28} p_{29} p_{30} \vee \ . \ . \ . \ \vee c_0 p_0 p_1 p_2$

$p_3 \ldots p_{29} p_{30}$

By using tree of smaller (e.g., 4-bit) carry-lookahead adders speed is traded-off for area and power

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32-input AND

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High fan-ins necessitate tree-structured circuits

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No circuit sharing: Repeated computations

32-input AND

32-input OR

High fan-ins necessitate tree-structured circuits

By using tree of smaller (e.g., 4-bit) carry-lookahead adders speed is traded-off for area and power

Basic multiplication operation

Shift/Add Multiplication Algorithms

Basic multiplication operation

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Notation for our discussion of multiplication algorithms:

a	Multiplicand	$a_{k-1}a_{k-2} \ldots a_1a_0$
x	Multiplier	$x_{k-1}x_{k-2} \ldots x_1x_0$
p	Product ($a \times x$)	$p_{2k-1}p_{2k-2} \ldots p_3p_2p_1p_0$

Initially, we assume unsigned operands

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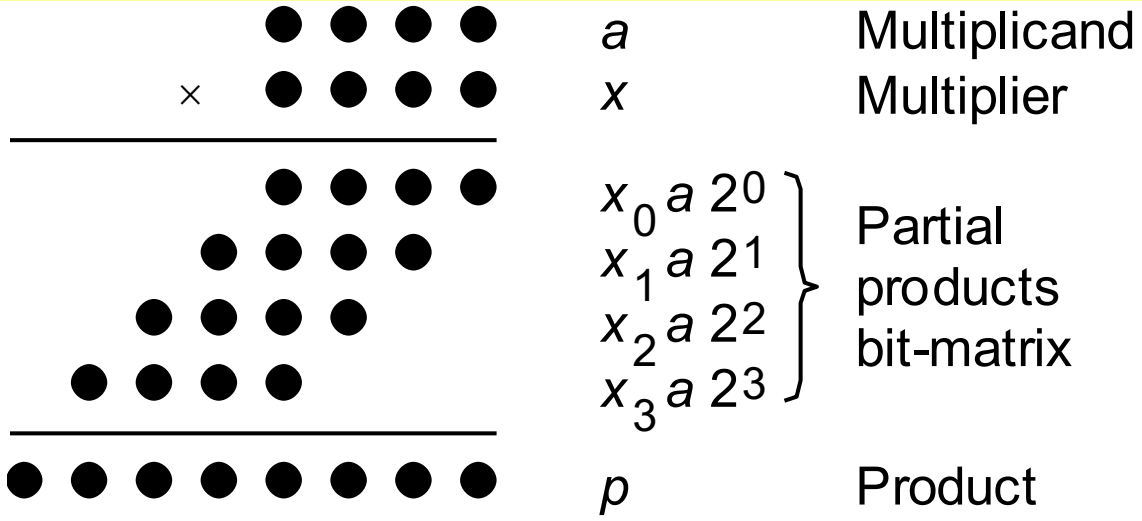
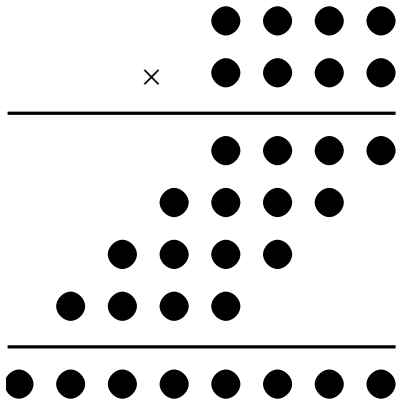


Multiplication of two 4-bit unsigned binary numbers in dot notation

Multiplication recurrence



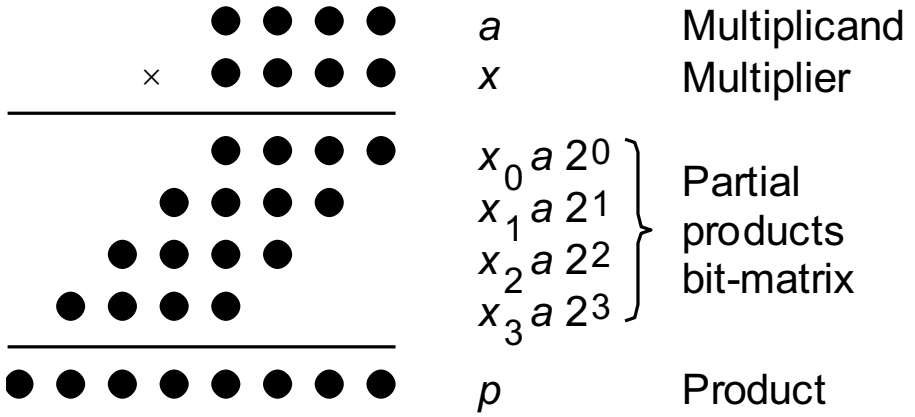
a Multiplicand

x Multiplier

$x_0\, a\, 2^0$
$x_1\, a\, 2^1$
$x_2\, a\, 2^2$
$x_3\, a\, 2^3$
} Partial products bit-matrix

p Product

Multiplication recurrence



Multiplication with left shifts: bottom-to-top accumulation

$$p^{(j+1)} = 2\,p^{(j)} + x_{k-j-1}a$$

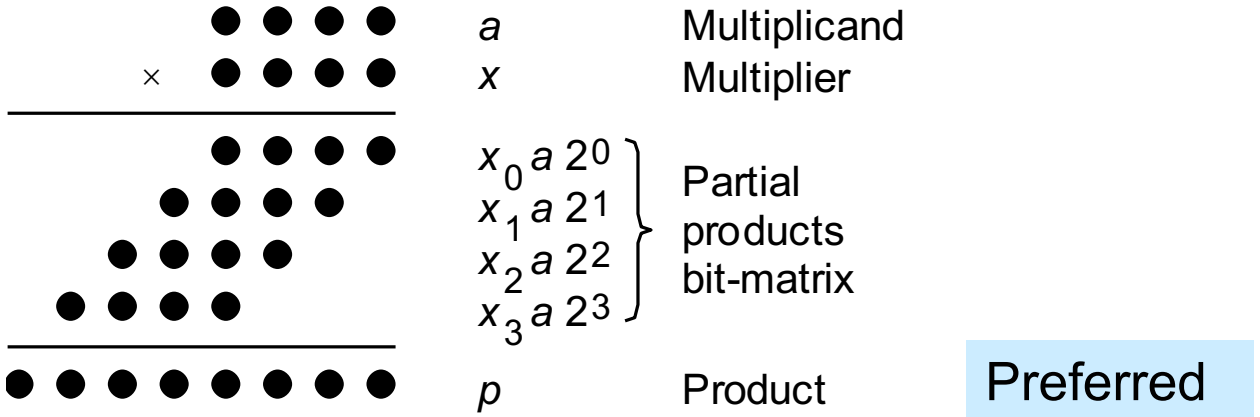
|shift|

|——add——|

with $p^{(0)} = 0$ and

$p^{(k)} = p = ax + p^{(0)}2^k$

Multiplication recurrence



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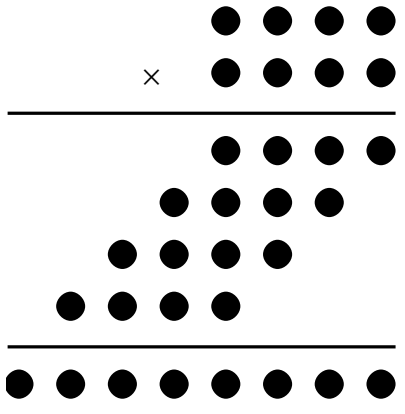

a Multiplicand
x Multiplier
$x_0\, a\, 2^0$
$x_1\, a\, 2^1$
$x_2\, a\, 2^2$
$x_3\, a\, 2^3$
Partial products bit-matrix
p Product

Preferred

Multiplication with right shifts: top-to-bottom accumulation

$$p^{(j+1)} = (p^{(j)} + x_j\, a\, 2^k)\, 2^{-1}$$

|——add——|
|—shift right—|

with $p^{(0)} = 0$ and
$p^{(k)} = p = ax + p^{(0)}2^{-k}$

Multiplication with left shifts: bottom-to-top accumulation

$$p^{(j+1)} = 2\,p^{(j)} + x_{k-j-1}a$$

|shift|
|——add——|

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Basic multiplication: example

Right-shift algorithm

a				1	0	1	0	
x				1	0	1	1	
$p^{(0)}$		0	0	0	0			
$+x_0a$		1	0	1	0			
$2p^{(1)}$	0	1	0	1	0			
$p^{(1)}$		0	1	0	1	0		
$+x_1a$		1	0	1	0			
$2p^{(2)}$	0	1	1	1	1	0		
$p^{(2)}$		0	1	1	1	1	0	
$+x_2a$		0	0	0	0			
$2p^{(3)}$	0	0	1	1	1	1	0	
$p^{(3)}$		0	0	1	1	1	1	0
$+x_3a$		1	0	1	0			
$2p^{(4)}$	0	1	1	0	1	1	1	0
$p^{(4)}$		0	1	1	0	1	1	1	0

Left-shift algorithm

a				1	0	1	0	
x				1	0	1	1	
$p^{(0)}$				0	0	0	0	
$2p^{(0)}$			0	0	0	0	0	
$+x_3a$				1	0	1	0	
$p^{(1)}$			0	1	0	1	0	
$2p^{(1)}$		0	1	0	1	0	0	
$+x_2a$				0	0	0	0	
$p^{(2)}$			0	1	0	1	0	0
$2p^{(2)}$		0	1	0	1	0	0	0
$+x_1a$				1	0	1	0	
$p^{(3)}$		0	1	1	0	0	1	0
$2p^{(3)}$	0	1	1	0	0	1	0	0
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Examples of sequential multiplication with right and left shifts.

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$p^{(2)}$		0	1	1	1	1	0	
$+x_2 a$		0	0	0	0			
$2p^{(3)}$	0	0	1	1	1	1	0	
$p^{(3)}$		0	0	1	1	1	1	0
$+x_3 a$		1	0	1	0			
$2p^{(4)}$	0	1	1	0	1	1	1	0
$p^{(4)}$		0	1	1	0	1	1	1	0

Left-shift algorithm

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$p^{(4)}$	0	1	1	0	1	1	1	0

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|——add——|

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$p^{(3)}$		0	0	1	1	1	1	0
$+x_3 a$				1	0	1	0	
$2p^{(4)}$	0	1	1	0	1	1	1	0
$p^{(4)}$		0	1	1	0	1	1	1	0

Left-shift algorithm

a					1	0	1	0
x					1	0	1	1
$p^{(0)}$					0	0	0	0
$2p^{(0)}$				0	0	0	0	0
$+x_3 a$					1	0	1	0
$p^{(1)}$				0	1	0	1	0
$2p^{(1)}$			0	1	0	1	0	0
$+x_2 a$					0	0	0	0
$p^{(2)}$			0	1	0	1	0	0
$p^{(4)}$		0	1	1	0	1	1	1	0

$$p^{(j+1)} = (p^{(j)} + x_j\, a\, 2^k)\, 2^{-1}$$

add

shift right

Examples of sequential multiplication with right and left shifts.

Basic multiplication: example

Right-shift algorithm

a					1	0	1	0
x	1	0	1	0	1	0	1	1
$p^{(0)}$				0	0	0	0	
$+x_0 a$				1	0	1	0	
$2p^{(1)}$			0	1	0	1	0	
$p^{(1)}$				0	1	0	1	0
$+x_1 a$				1	0	1	0	
$2p^{(2)}$		0	1	1	1	1	0	
$p^{(2)}$			0	1	1	1	1	0
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$p^{(3)}$		0	0	1	1	1	1	0
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|——add——|

|—shift right—|

Examples of sequential multiplication with right and left shifts.

Check:
10×11
$= 110$
$= 64 + 32 + 8 + 4 + 2$

Basic multiplication: example

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x					1	0	1	1
$p^{(0)}$		0	0	0	0			
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$2p^{(1)}$	0	1	0	1	0			
$p^{(1)}$		0	1	0	1	0		
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$2p^{(2)}$	0	1	1	1	1	0		
$p^{(2)}$		0	1	1	1	1	0	
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$2p^{(3)}$	0	0	1	1	1	1	0	
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a					1	0	1	0
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$p^{(0)}$					0	0	0	0
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$+x_2a$					0	0	0	0
$p^{(2)}$			0	1	0	1	0	0
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$p^{(3)}$		0	1	1	0	0	1	0
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Basic multiplication: example

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$p^{(0)}$		0	0	0	0			
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$p^{(j+1)} = 2\,p^{(j)} + x_{k-j-1}\,a$

|shift|

|——add——|

Left-shift algorithm

a					1	0	1	0
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$p^{(0)}$					0	0	0	0
$2p^{(0)}$			0	0	0	0	0	
$+x_3 a$					1	0	1	0
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$p^{(2)}$		0	1	0	1	0	0	
$2p^{(2)}$	0	1	0	1	0	0	0	
$+x_1 a$					1	0	1	0
$p^{(3)}$	0	1	1	0	0	1	0	
$2p^{(3)}$	0	1	1	0	0	1	0	0
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Examples of sequential multiplication with right and left shifts.

Basic multiplication: example

Right-shift algorithm

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$p^{(0)}$			0	0	0	0		
$+x_0 a$			1	0	1	0		
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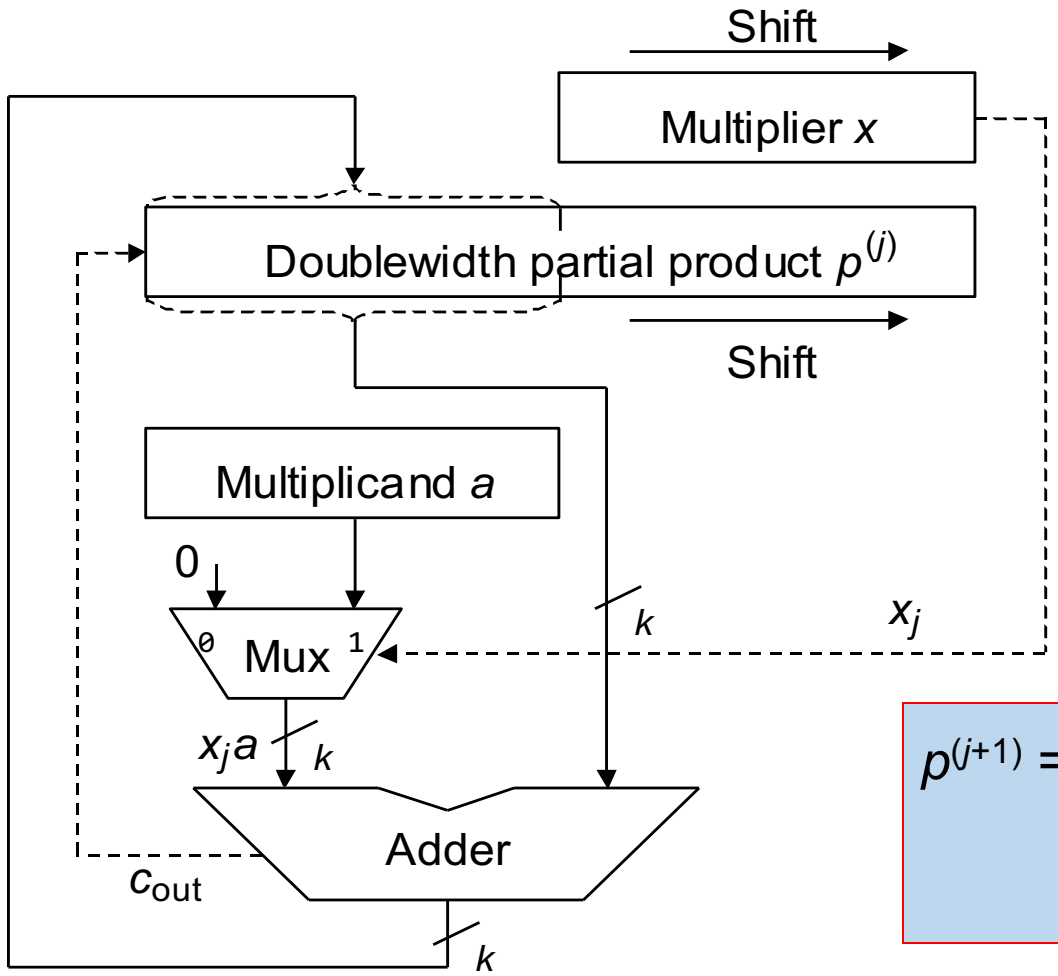
$+x_2 a$					0	0	0	0
$p^{(2)}$		0	1	0	1	0	0	
$2p^{(2)}$	0	1	0	1	0	0	0	
$+x_1 a$					1	0	1	0
$p^{(3)}$		0	1	1	0	0	1	0
$2p^{(3)}$	0	1	1	0	0	1	0	0
$+x_0 a$					1	0	1	0
$p^{(4)}$		0	1	1	0	1	1	1	0

Examples of sequential multiplication with right and left shifts.

Check:
10×11
$= 110$
$= 64 + 32 + 8 + 4 + 2$

Basic multiplier: hardware implementation



$$p^{(j+1)} = (p^{(j)} + x_j\, a\, 2^k)\, 2^{-1}$$
$$\text{add}$$
$$\text{shift right}$$

Hardware realization of the sequential multiplication algorithm with additions and right shifts

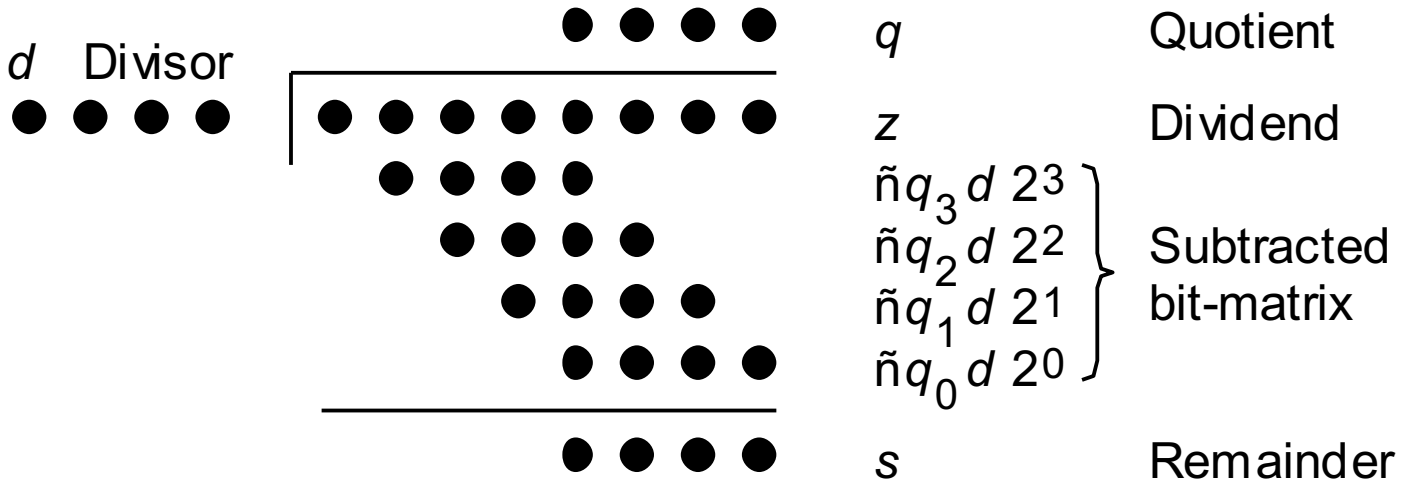
Basic division operation

Division algorithm based on the pen and paper approach

Notation for our discussion of division algorithms:

z	Dividend	$z_{2k-1}z_{2k-2} \ . \ . \ . \ z_3z_2z_1z_0$
d	Divisor	$d_{k-1}d_{k-2} \ldots d_1d_0$
q	Quotient	$q_{k-1}q_{k-2} \ldots q_1q_0$
s	Remainder, $z - (d \times q)$	$s_{k-1}s_{k-2} \ldots s_1s_0$

Initially, we assume unsigned operands

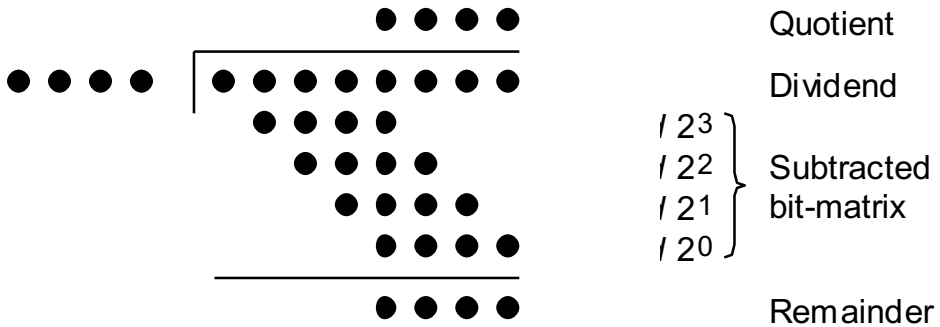


Division of an 8-bit number by a 4-bit number in dot notation

Division versus multiplication

Division is more complex than multiplication:
- Need for quotient digit selection or estimation

Overflow possibility: the high-order *k* bits of *z* must be strictly less than *d*; this overflow check also detects the divide-by-zero condition.



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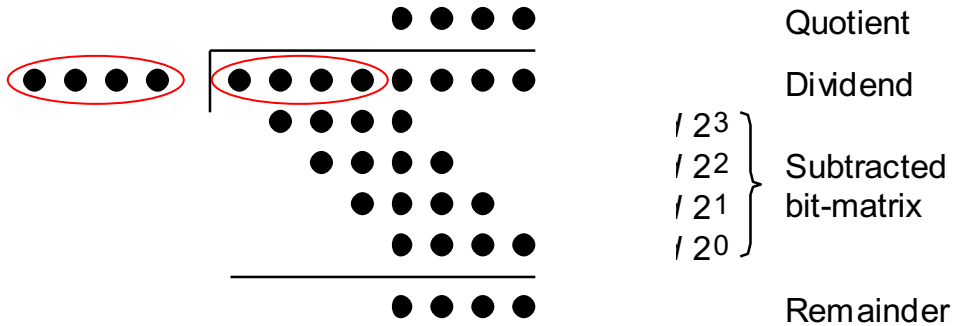

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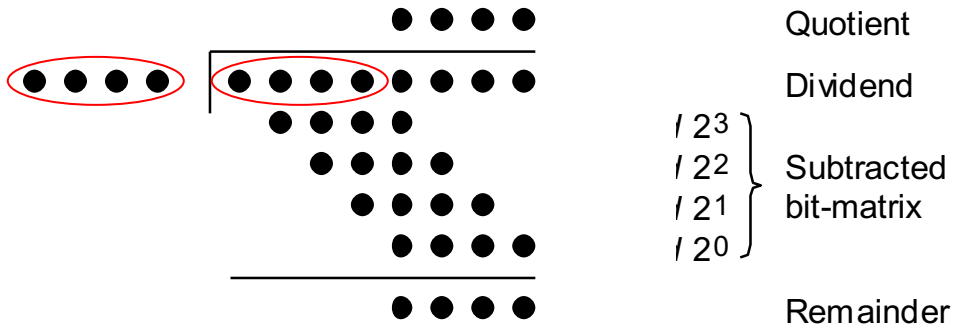

Pentium III latencies

Instruction	Latency	Cycles/Issue
Load / Store	3	1
Integer Multiply	4	1
Integer Divide	36	36
Double/Single FP Multiply	5	2
Double/Single FP Add	3	1
Double/Single FP Divide	38	38

Division versus multiplication

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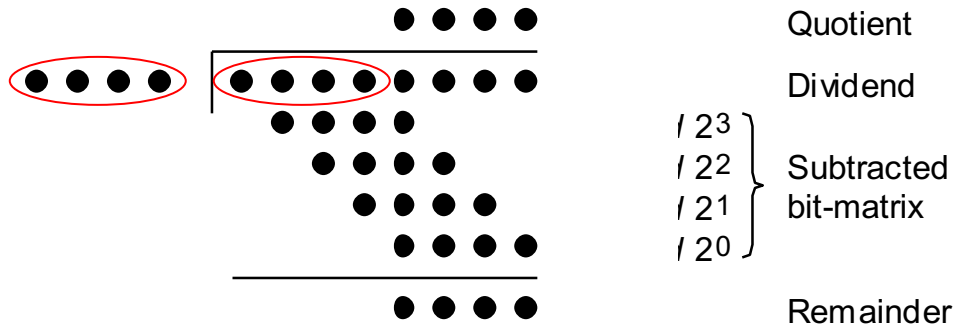

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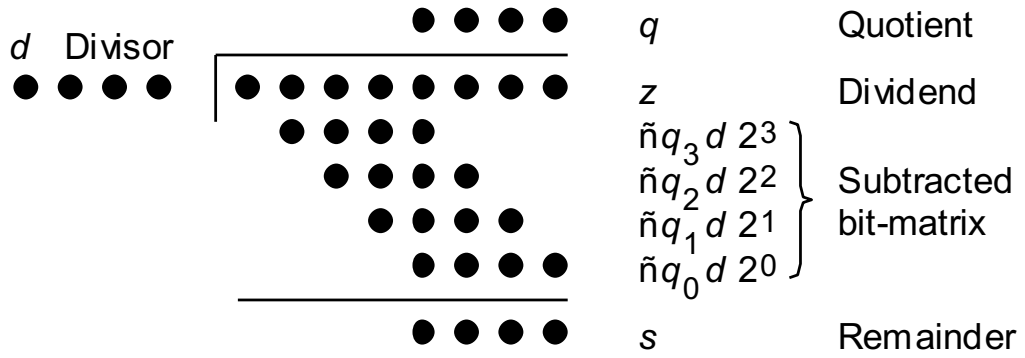
Double/Single FP Add	3	1
Double/Single FP Divide	38	38

The ratios haven't changed much in later Pentiums, Atom, or AMD products*

*Source: T. Granlund, "Instruction Latencies and Throughput for AMD and Intel x86 Processors," Feb. 2012

Division by recurrence: slow division



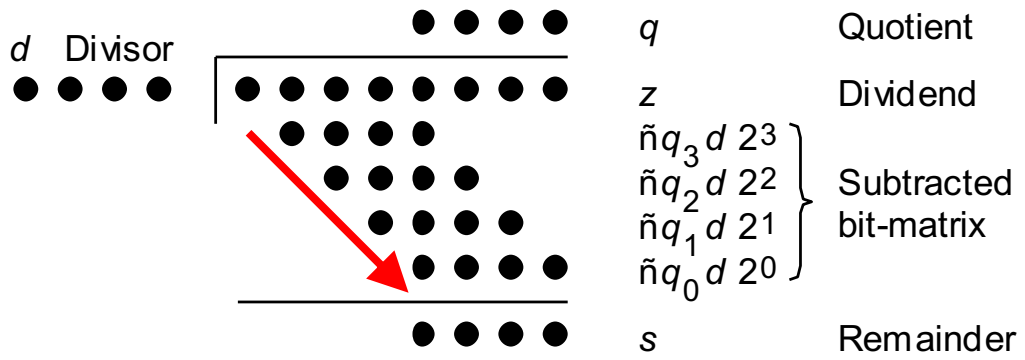
Division with left shifts

$$s^{(j)} = 2s^{(j-1)} - q_{k-j}(2^k d)$$

|–shift–|
|——subtract——|

with $s^{(0)} = z$ and $s^{(k)} = 2^k s$

Division by recurrence: slow division



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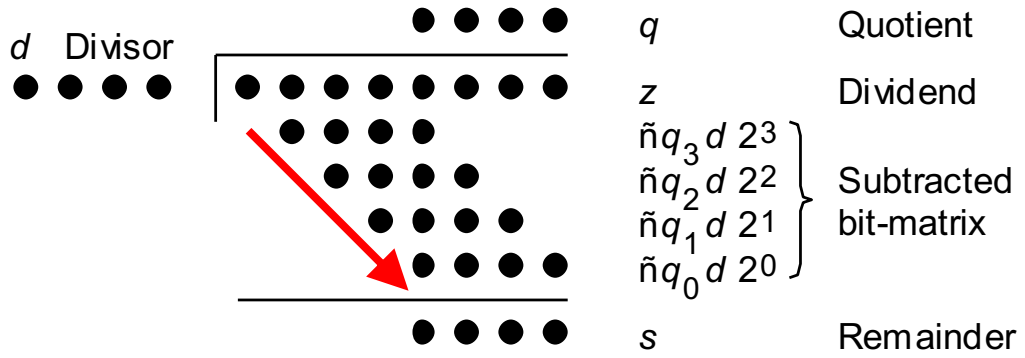

Division with left shifts (There is no corresponding right-shift algorithm)

$$s^{(j)} = 2s^{(j-1)} - q_{k-j}(2^k d)$$

|–shift–|

|——subtract——|

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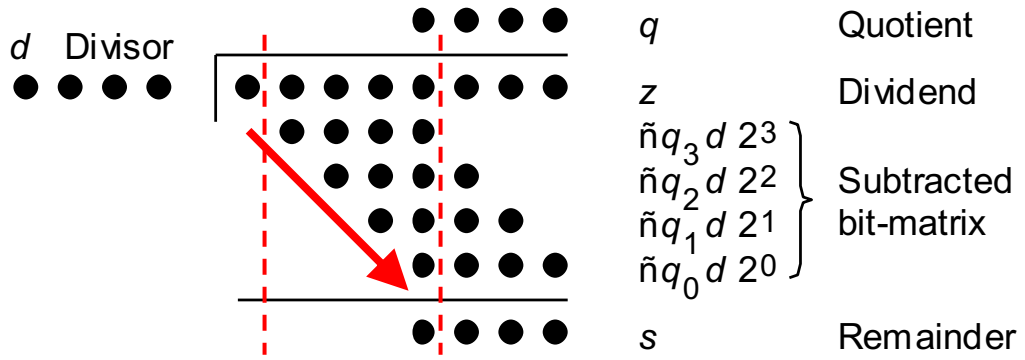
Division by recurrence: slow division



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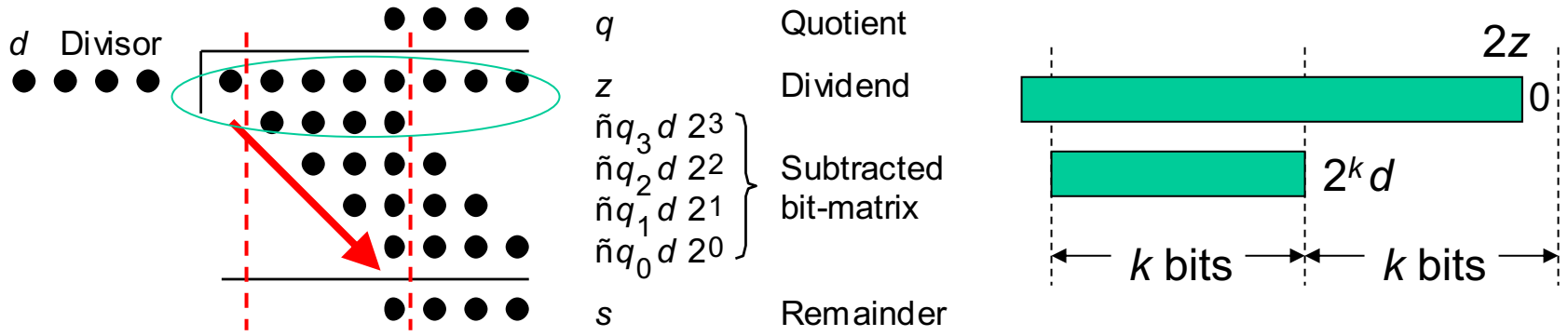

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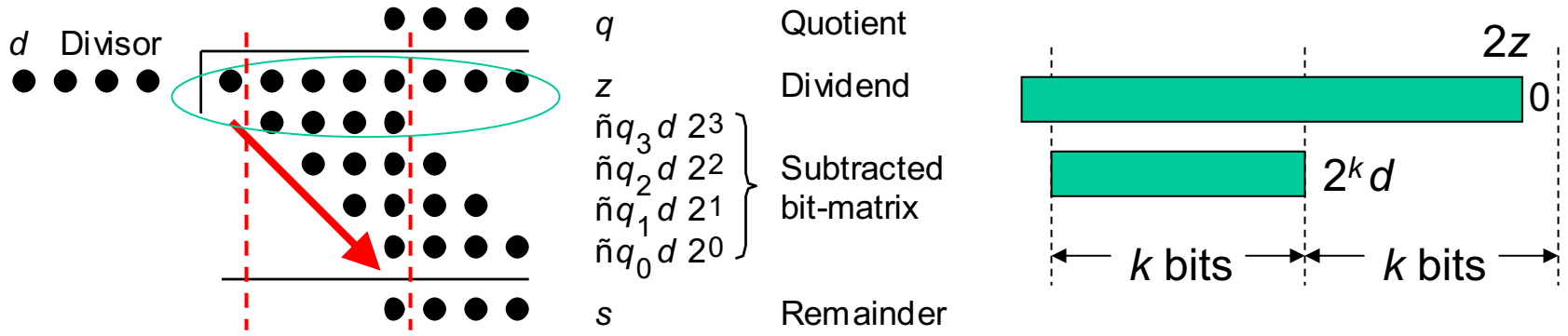

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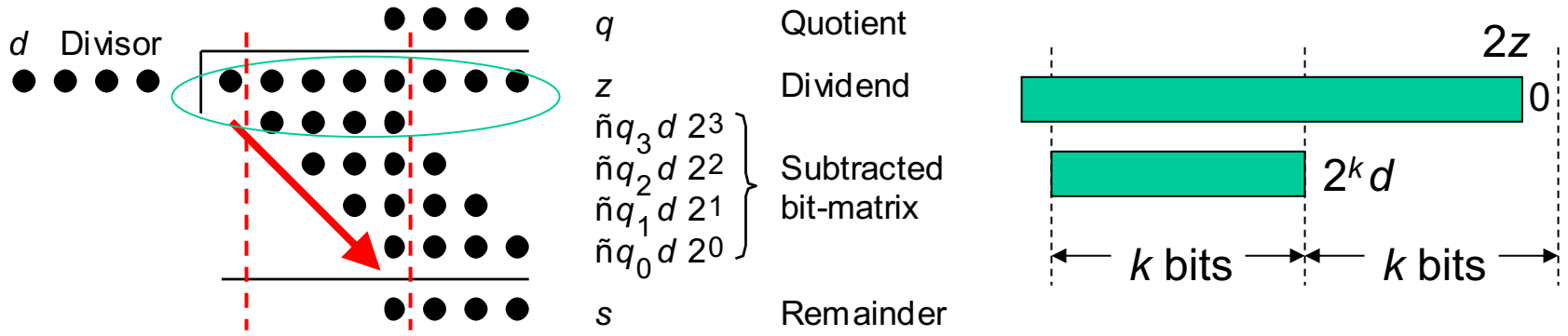
Integer division is characterized by $z = d \times q + s$

$$2^{-2k}z = (2^{-k}d) \times (2^{-k}q) + 2^{-2k}s$$

$$z_{frac} = d_{frac} \times q_{frac} + 2^{-k}s_{frac}$$

Divide fractions like integers; adjust the remainder

Division by recurrence: slow division



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$$2^{-2k}z = (2^{-k}d) \times (2^{-k}q) + 2^{-2k}s$$

$$z_{frac} = d_{frac} \times q_{frac} + 2^{-k}s_{frac}$$

Divide fractions like integers; adjust the remainder

No-overflow condition for fractions is:

$z_{frac} < d_{frac}$

Example of basic division

Integer division

z		0	1	1	1	0	1	0 1
$2^4 d$		1	0	1	0			
$s^{(0)}$		0	1	1	1	0	1	0 1
$2s^{(0)}$	0	1	1	1	0	1	0	1
$-q_3 2^4 d$		1	0	1	0			$\{q_3 = 1\}$

Fractional division

z_{frac}		.	0	1	1	1	0	1 0 1
d_{frac}		.	1	0	1	0		
$s^{(0)}$		.	0	1	1	1	0	1 0 1
$2s^{(0)}$	0	.	1	1	1	0	1	0 1
$-q_{-1} d$		.	1	0	1	0		$\{q_{-1}=1\}$

Examples of sequential division with integer and fractional operands.

Example of basic division

Decimal

Integer division

z	117	0 1 1 1 0 1 0 1
$2^4 d$		1 0 1 0
$s^{(0)}$		0 1 1 1 0 1 0 1
$2s^{(0)}$		0 1 1 1 0 1 0 1
$-q_3 2^4 d$		1 0 1 0 {$q_3 = 1$}

Fractional division

z_{frac}	. 0 1 1 1 0 1 0 1
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Examples of sequential division with integer and fractional operands.

Example of basic division

Decimal

Integer division

z	117	0 1 1 1 0 1 0 1
$2^4 d$	10	1 0 1 0
$s^{(0)}$		0 1 1 1 0 1 0 1
$2s^{(0)}$		0 1 1 1 0 1 0 1
$-q_3 2^4 d$		1 0 1 0 {$q_3 = 1$}

Fractional division

z_{frac}	. 0 1 1 1 0 1 0 1
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$-q_2 2^4 d$		0 0 0 0 $\{q_2 = 0\}$

Fractional division

z_{frac}	. 0 1 1 1 0 1 0 1
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$s^{(2)}$		1 0 0 1 0 1
$2s^{(2)}$		1 0 0 1 0 1
$-q_1 2^4 d$		1 0 1 0 $\{q_1 = 1\}$

Fractional division

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$2s^{(1)}$		0 1 0 0 1 0 1
$-q_2 2^4 d$		0 0 0 0 $\{q_2 = 0\}$
$s^{(2)}$		1 0 0 1 0 1
$2s^{(2)}$		1 0 0 1 0 1
$-q_1 2^4 d$		1 0 1 0 $\{q_1 = 1\}$
$s^{(3)}$		1 0 0 0 1
$2s^{(3)}$		1 0 0 0 1
$-q_0 2^4 d$		1 0 1 0 $\{q_0 = 1\}$

Fractional division

z_{frac}	. 0 1 1 1 0 1 0 1
d_{frac}	. 1 0 1 0
$s^{(0)}$	. 0 1 1 1 0 1 0 1
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$s^{(1)}$	. 0 1 0 0 1 0 1
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$-q_2 2^4 d$		0 0 0 0 $\{q_2 = 0\}$
$s^{(2)}$		1 0 0 1 0 1
$2s^{(2)}$		1 0 0 1 0 1
$-q_1 2^4 d$		1 0 1 0 $\{q_1 = 1\}$
$s^{(3)}$		1 0 0 0 1
$2s^{(3)}$		1 0 0 0 1
$-q_0 2^4 d$		1 0 1 0 $\{q_0 = 1\}$
$s^{(4)}$		0 1 1 1
s		0 1 1 1
q		1 0 1 1

Fractional division

z_{frac}	. 0 1 1 1 0 1 0 1
d_{frac}	. 1 0 1 0
$s^{(0)}$	. 0 1 1 1 0 1 0 1
$2s^{(0)}$	0 . 1 1 1 0 1 0 1
$-q_{-1} d$	. 1 0 1 0 $\{q_{-1}=1\}$
$s^{(1)}$	. 0 1 0 0 1 0 1
$2s^{(1)}$	0 . 1 0 0 1 0 1
$-q_{-2} d$	. 0 0 0 0 $\{q_{-2}=0\}$
$s^{(2)}$	. 1 0 0 1 0 1
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$s^{(4)}$	. 0 1 1 1
s_{frac}	0 . 0 0 0 0 0 1 1 1
q_{frac}	. 1 0 1 1

Examples of sequential division with integer and fractional operands.

Example of basic division

Decimal

Integer division

z	117	0 1 1 1 0 1 0 1
$2^4 d$	10	1 0 1 0
$s^{(0)}$		0 1 1 1 0 1 0 1
$2s^{(0)}$		0 1 1 1 0 1 0 1
$-q_3 2^4 d$		1 0 1 0 $\{q_3 = 1\}$
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s	7	0 1 1 1
q	11	1 0 1 1

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No finite number system can represent all real numbers
Various systems can be used for a subset of real numbers

Fixed-point	$\pm w.f$
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A floating-point number comes with two signs:

Number sign, usually appears as a separate bit
Exponent sign, usually embedded in the biased exponent

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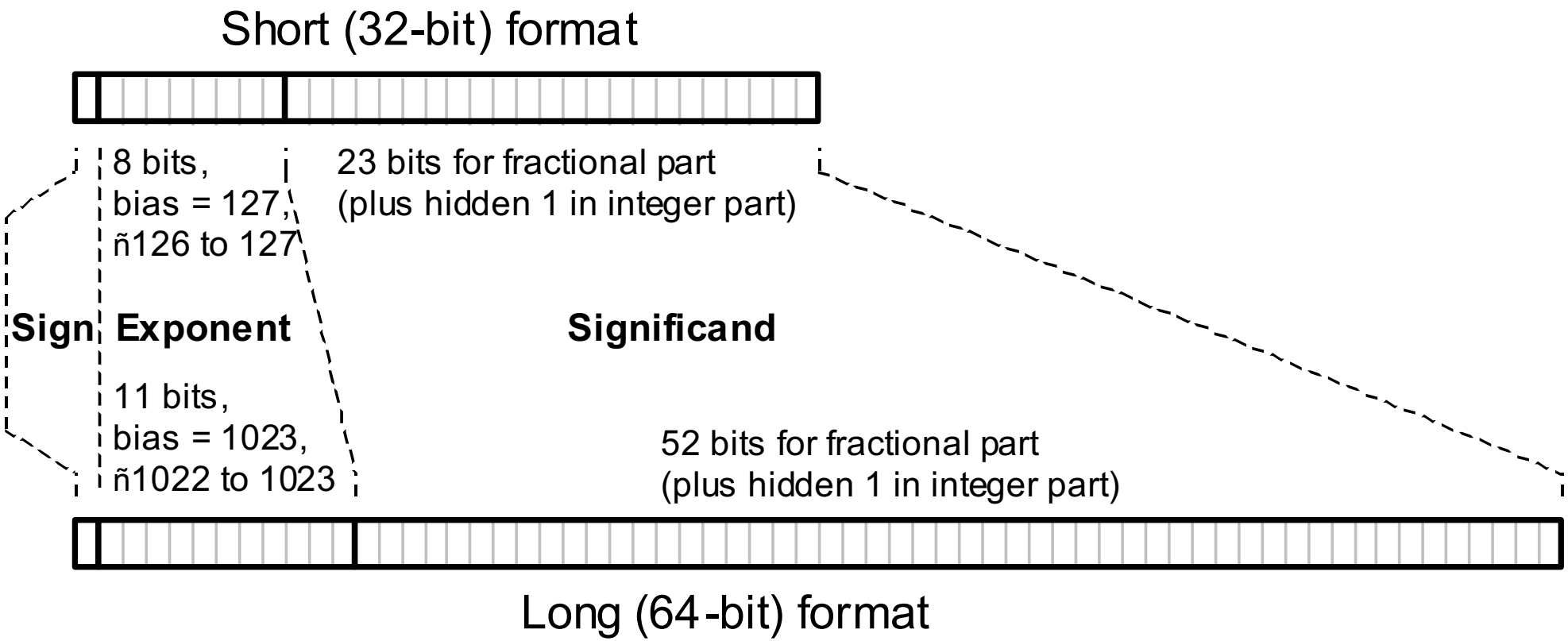
- First IEEE standard for binary floating-point arithmetic was adopted in 1985 after years of discussion
- The 1985 standard was continuously discussed, criticized, and clarified for a couple of decades
- In 2008, after several years of discussion, a revised standard was issued

The IEEE 754 floating point standard representation



The IEEE 754 standard floating-point number representation formats

Overview of IEEE 754 standard

Feature	Single / Short	Double / Long
Word width (bits)	32	64
Significand bits	23 + 1 hidden	52 + 1 hidden
Significand range	$[1, 2 - 2^{-23}]$	$[1, 2 - 2^{-52}]$
Exponent bits	8	11
Exponent bias	127	1023
Zero (± 0)	$e + bias = 0$, $f = 0$	$e + bias = 0$, $f = 0$
Denormal	$e + bias = 0$, $f \neq 0$	$e + bias = 0$, $f \neq 0$
	represents $\pm 0.f \times 2^{-126}$	represents $\pm 0.f \times 2^{-1022}$
Infinity ($\pm\infty$)	$e + bias = 255$, $f = 0$	$e + bias = 2047$, $f = 0$
Not-a-number (NaN).	$e + bias = 255$, $f \neq 0$	$e + bias = 2047$, $f \neq 0$
Ordinary number	$e + bias \in [1, 254]$	$e + bias \in [1, 2046]$
	$e \in [-126, 127]$	$e \in [-1022, 1023]$
	represents $1.f \times 2^e$	represents $1.f \times 2^e$
min	$2^{-126} \cong 1.2 \times 10^{-38}$	$2^{-1022} \cong 2.2 \times 10^{-308}$
max	$\cong 2^{128} \cong 3.4 \times 10^{38}$	$\cong 2^{1024} \cong 1.8 \times 10^{308}$

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- Special values
  - Zero ➔ all exponent and mantissa of 0 values-0 and +0 are equal
  - Denormalised ➔ exponent = 0 and mantissa ≠ 0, i.e., the number does not have leading 1 before the binary point
  - Infinity ➔ all exponent ‘1’ and all mantissa ‘0’. Sign bit 1 = -∞ and 0 = ∞
  - NAN ➔represents error value exponent all ‘1’ mantissa ≠ 0

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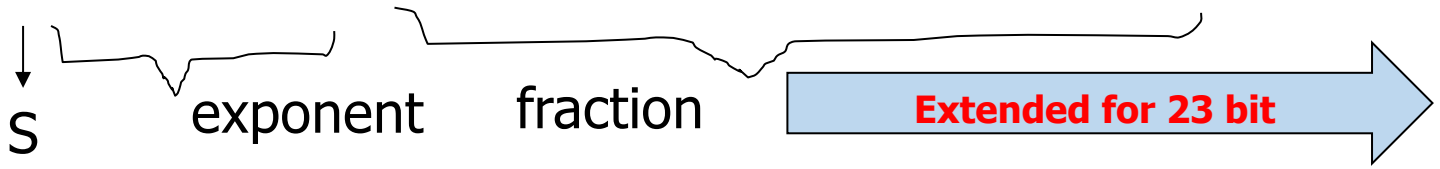

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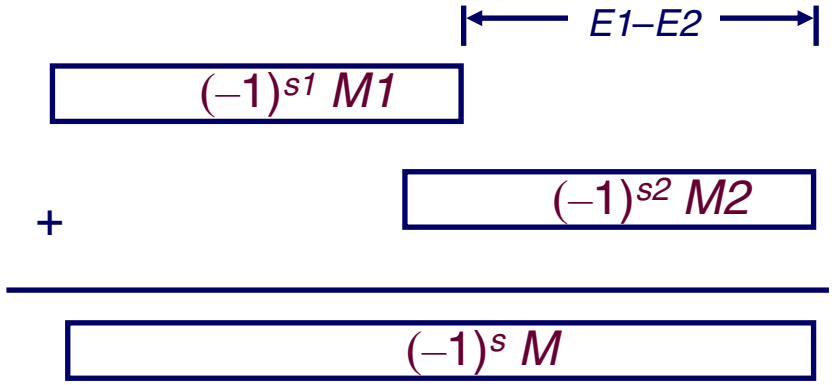

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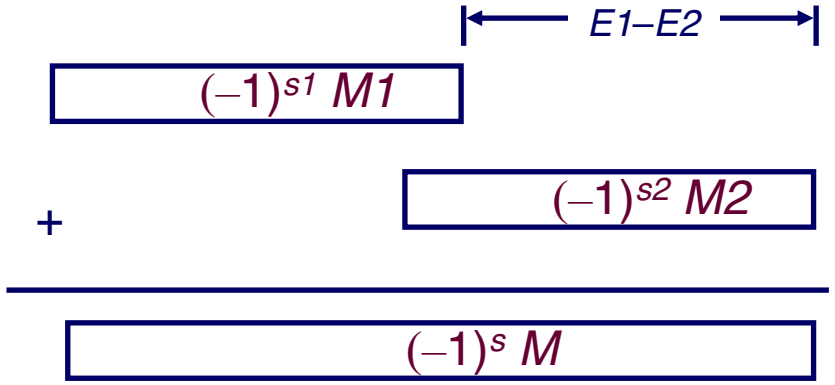

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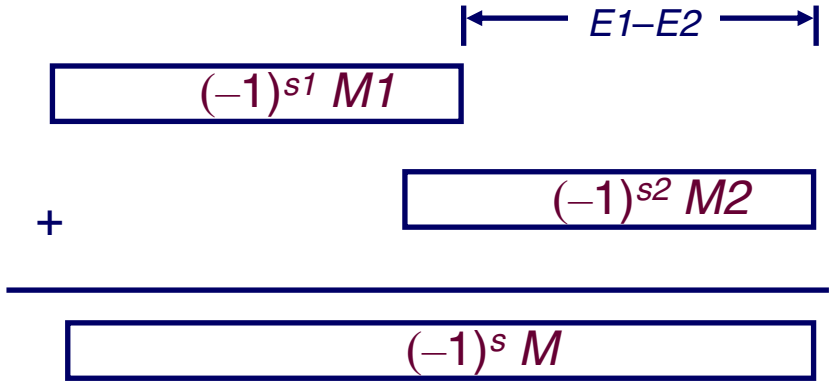

Fixing

- **If** $M \geq 2$**, shift** M **right 'k' positions, increment** E **by k**
- **if** $M < 1$**, shift** M **left '**k**' positions, decrement** E **by** k
- **Overflow if** E **out of range**
- **Round** M **to fit** `frac` **precision**

Floating point addition: example

- Complex operation when compared to integer

  Consider a 4-digit binary example

  $1.000_2 \times 2^{-1} + -1.110_2 \times 2^{-2}$ (0.5 + –0.4375)

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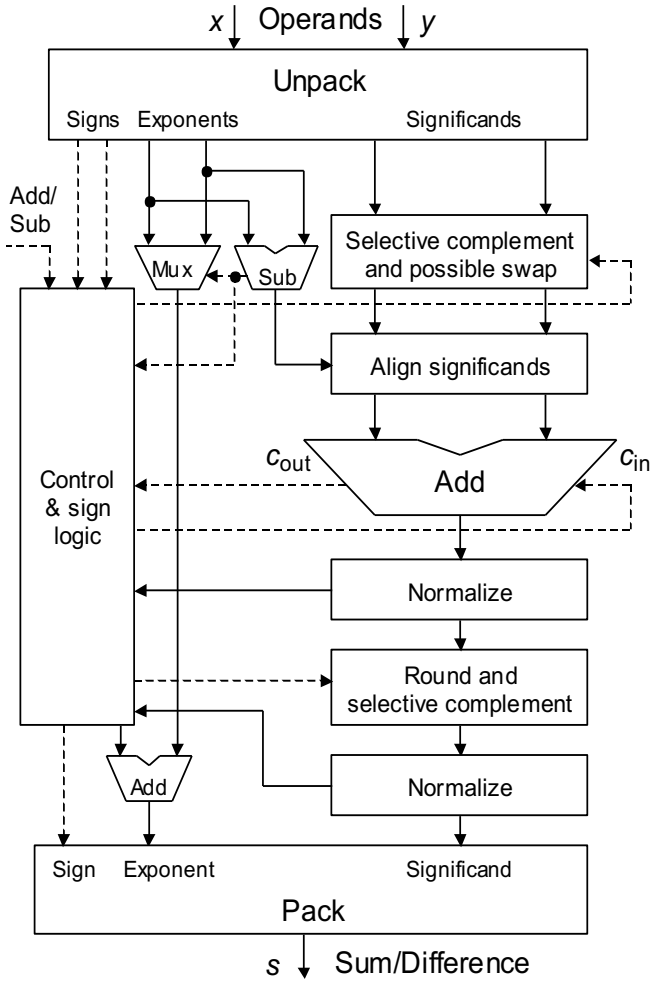
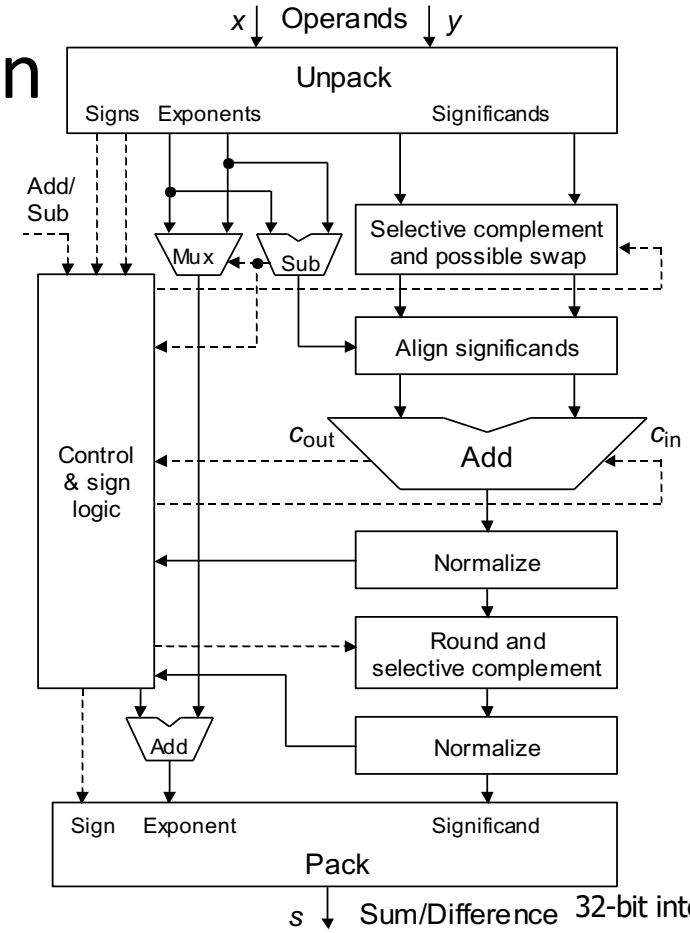


Floating point vs integer addition

Integer addition simple operation

- Handle carry
- Handle overflow



32-bit integer adder with carry skip adder blocks

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- Operand pre-processing
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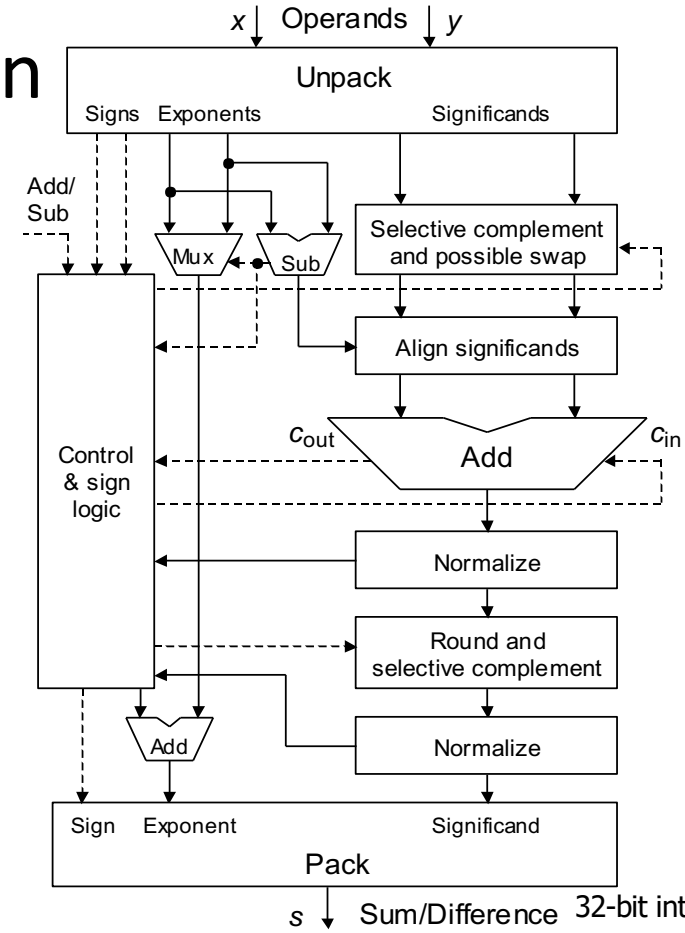

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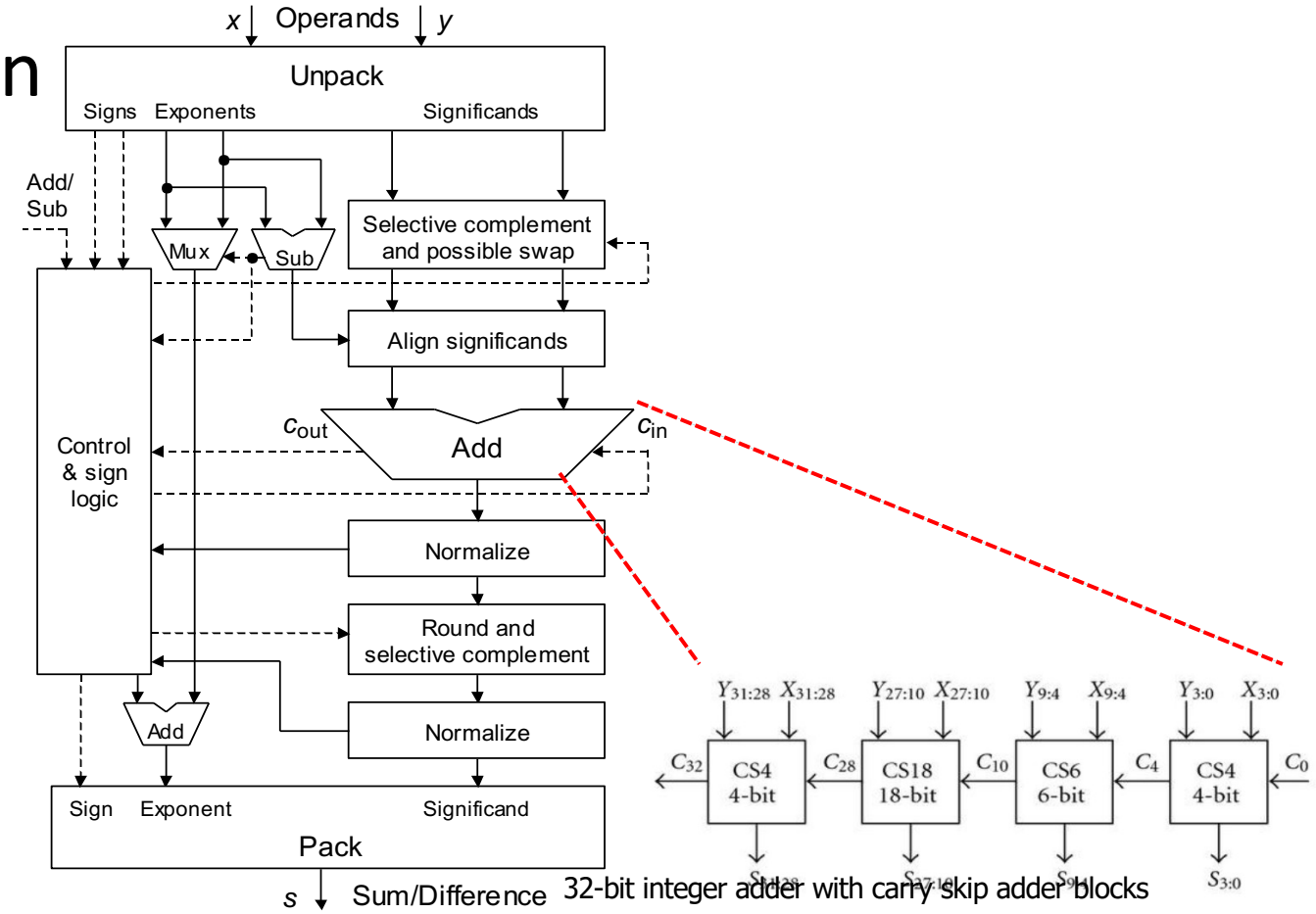

32-bit integer adder with carry skip adder blocks

Floating point multiplication

- **Operands**
  - $(-1)^{s1}\ M1\ \ 2^{E1}$ * $(-1)^{s2}\ M2\ \ 2^{E2}$
- **Exact Result**
  - $(-1)^{s}\ M\ \ 2^{E}$
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- **Implementation**
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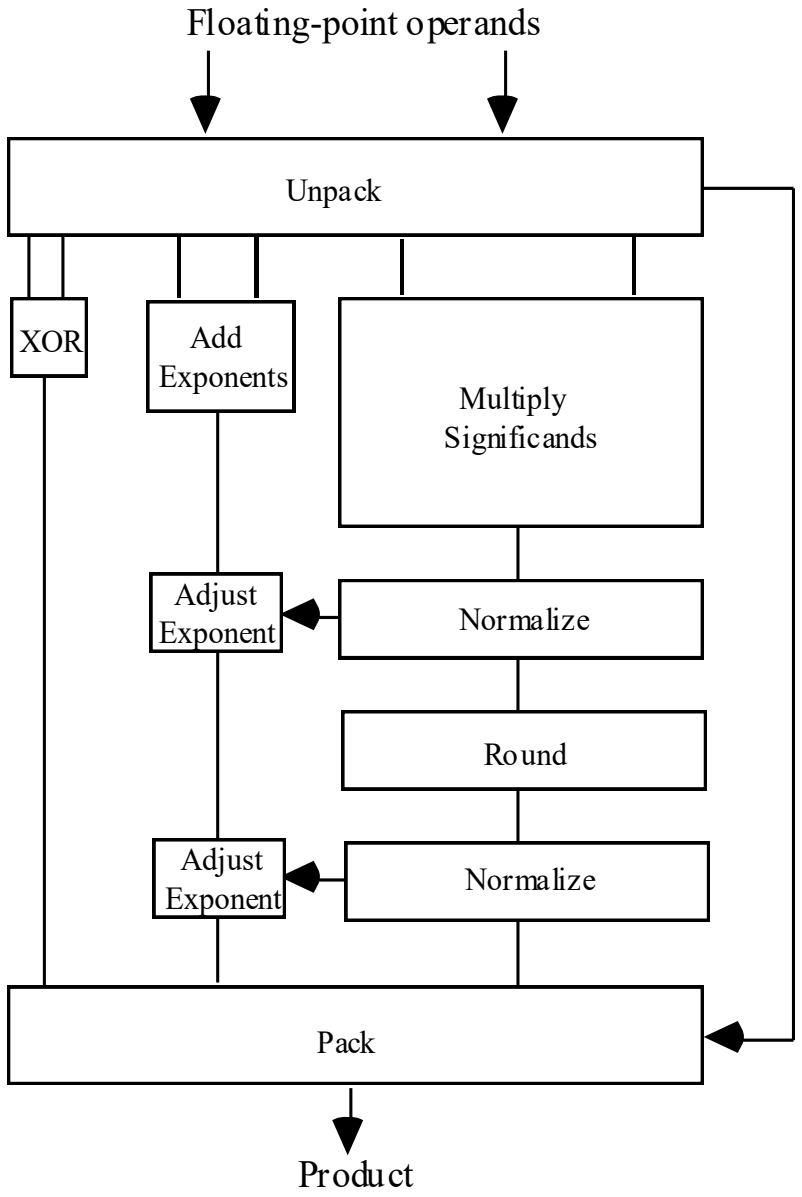
$$(\pm s1 \times b^{e1}) \times (\pm s2 \times b^{e2}) = (\pm s1 \times s2) \times b^{e1+e2}$$

$s1 \times s2 \in [1, 4)$: may need post-shifting



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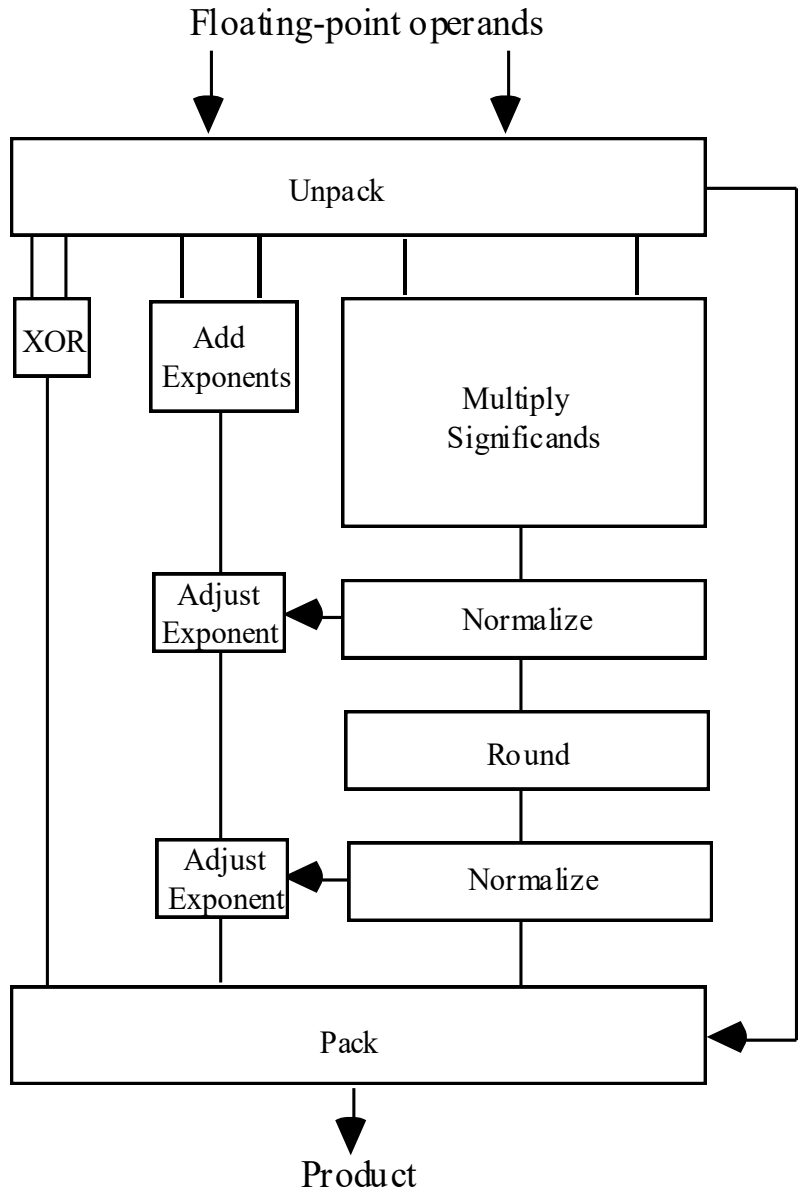

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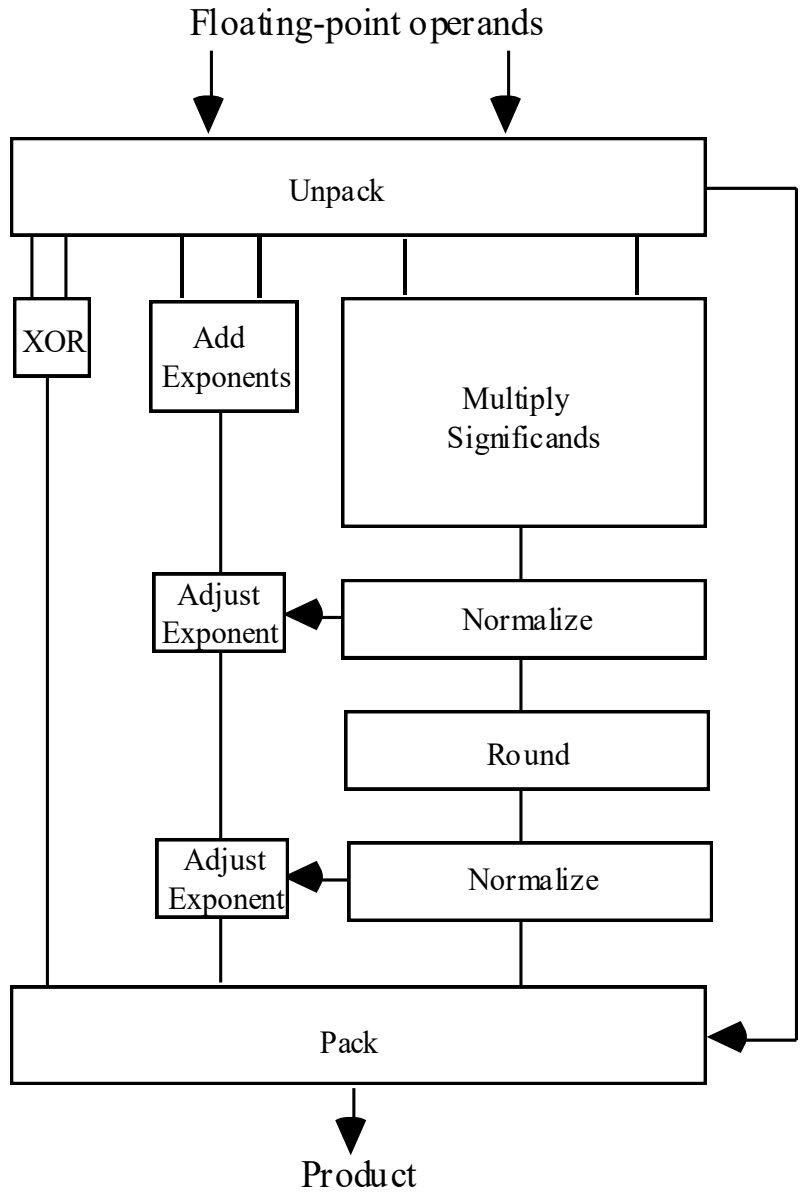
Considerations:

- Rounding and truncation
- Result normalization



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Divide by zero

Overflow

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Produce NaN as their results

Advanced cases: big problems in today's computing

- Too much energy and power needed per calculation
- Not enough bandwidth (the "memory wall")
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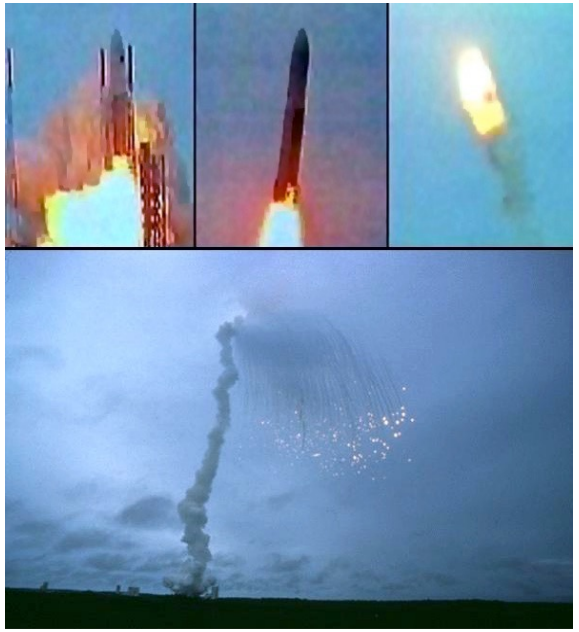
"The computer cannot give you the exact value, sorry. Use *this* value instead. It's close."



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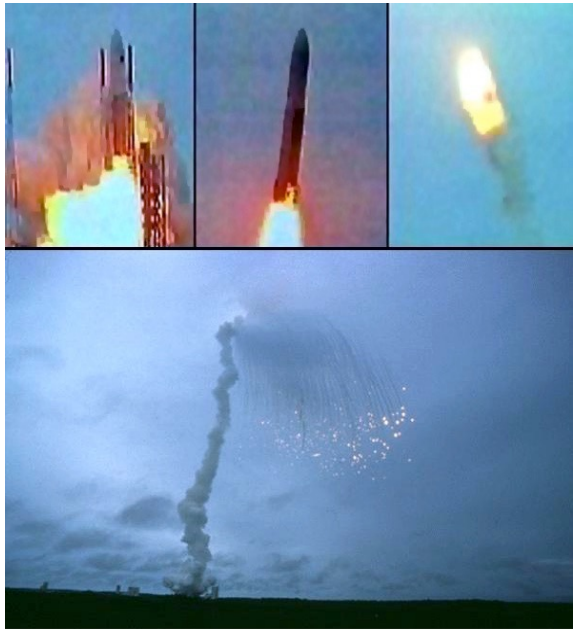

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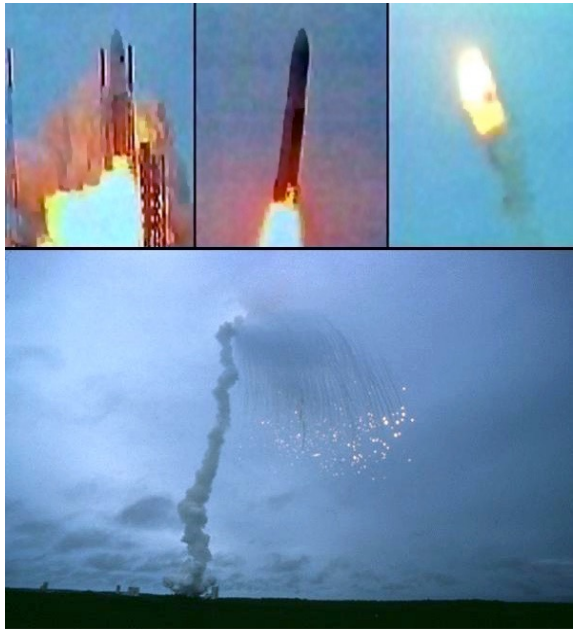

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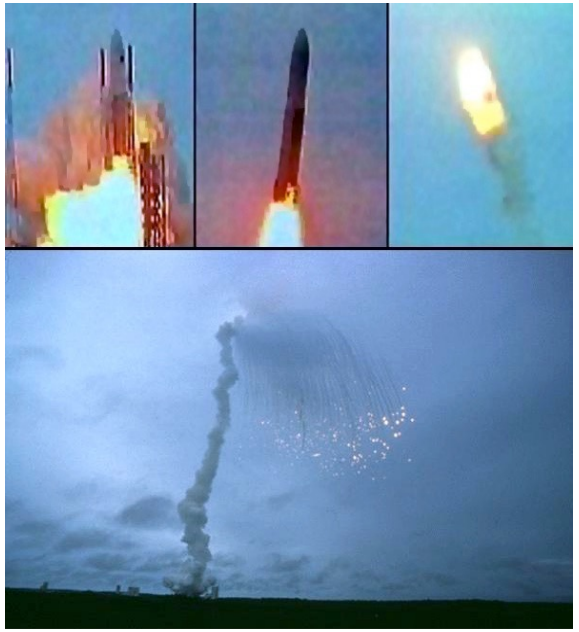

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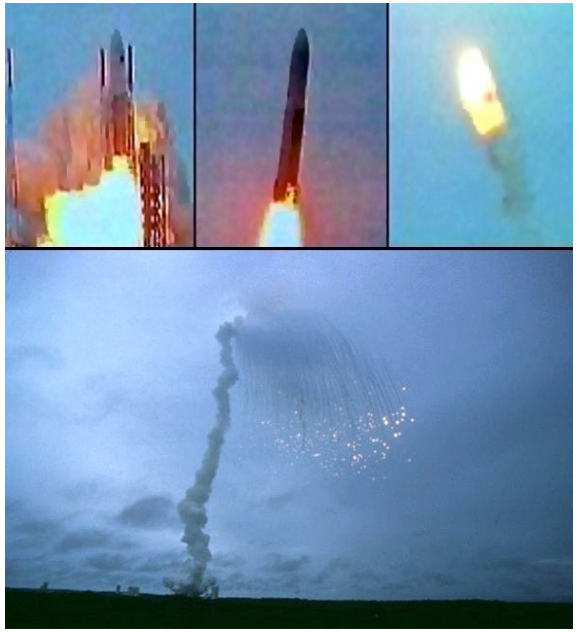

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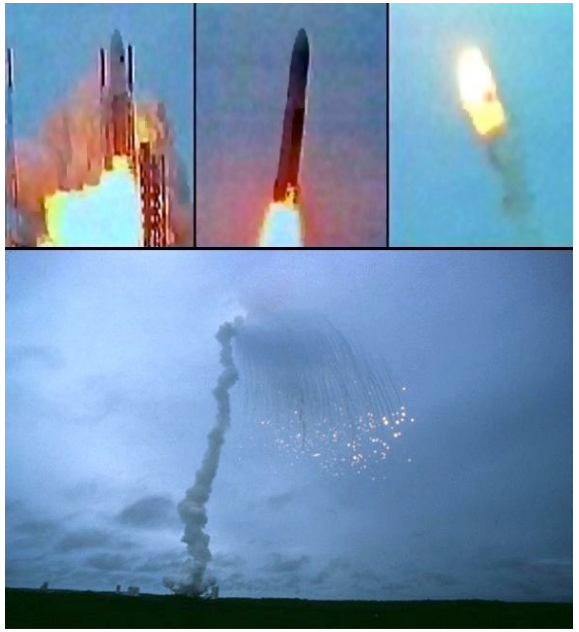

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What can we do? A new number format?

A New Number Format: The Unum

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"You can't boil the ocean."

—Former Intel exec, when shown the unum idea

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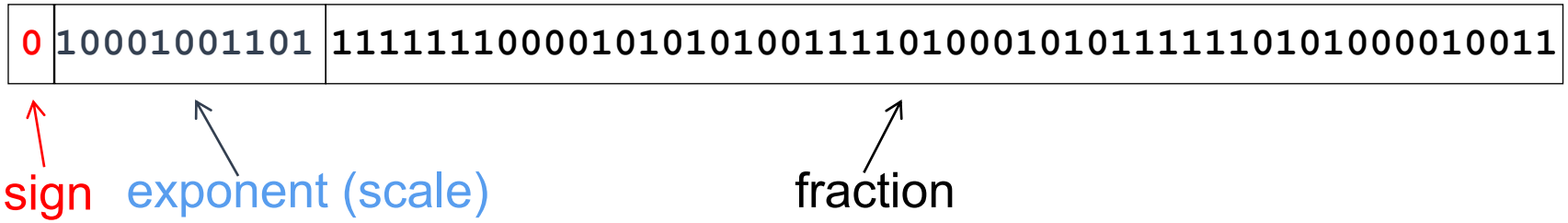
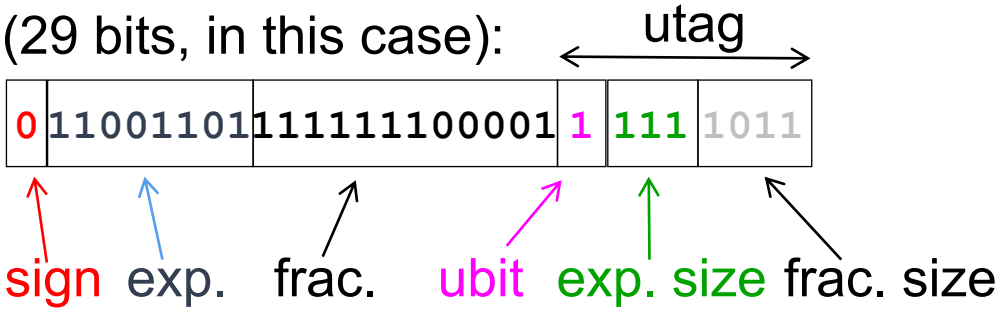
Unum basics: avoid the price of "one size fits all"

IEEE Standard Float (64 bits):



Self-descriptive "utag" bits track and manage uncertainty, exponent size, and fraction size

Unum
(29 bits, in this case):



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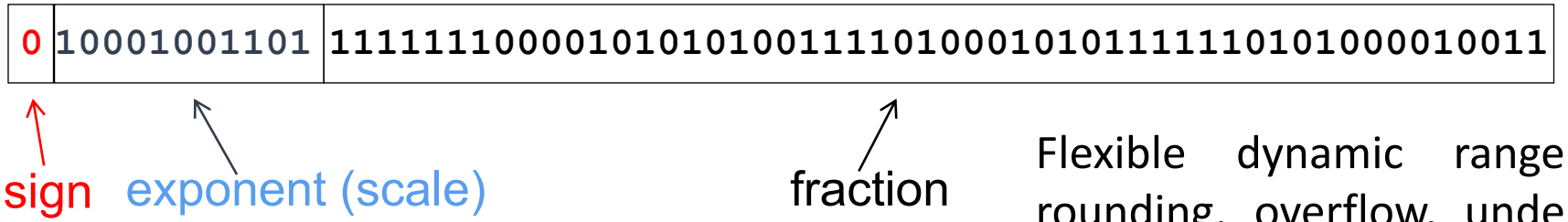

Flexible dynamic range Flexible precision No rounding, overflow, underflow No "negative zero" Fixes wasted NaN values Makes results bit-identical

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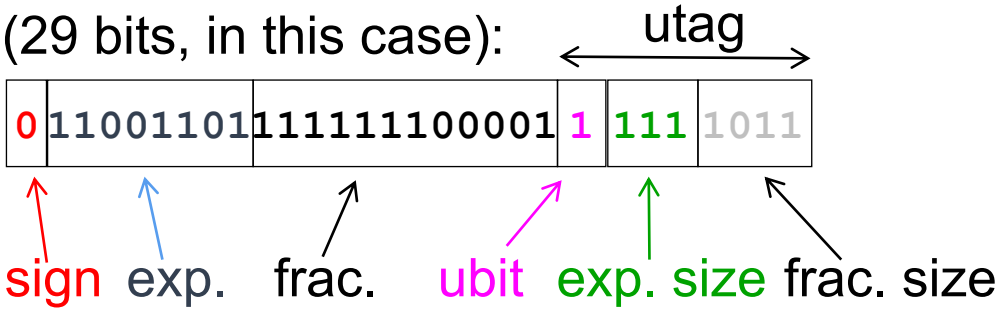

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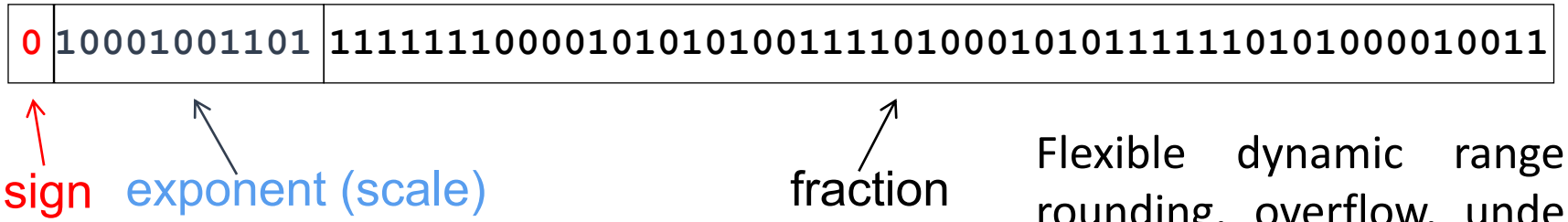

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BUT:

Variable storage size Adds indirection Many conditional tests

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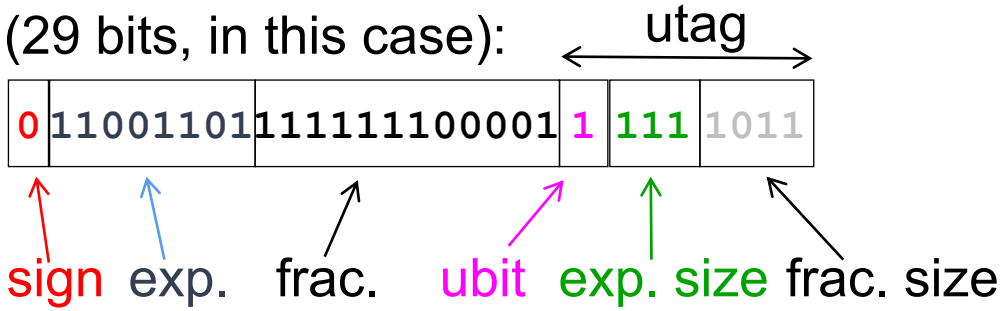
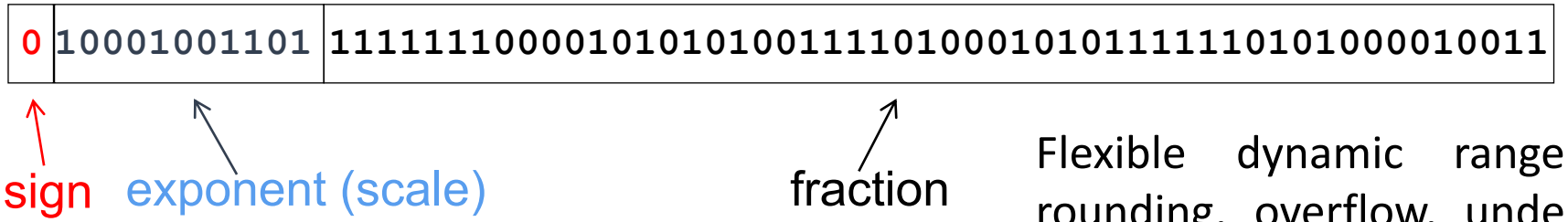


Unum basics: avoid the price of "one size fits all"

IEEE Standard Float (64 bits):



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Self-descriptive "utag" bits track and manage uncertainty, exponent size, and fraction size

BUT:

Variable storage size Adds indirection Many conditional tests

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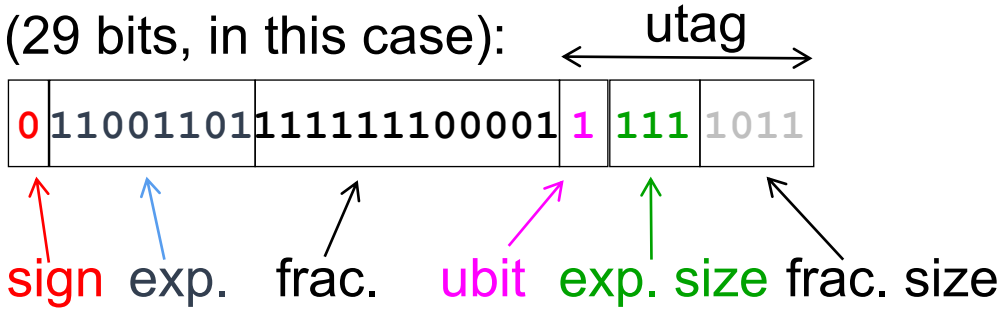


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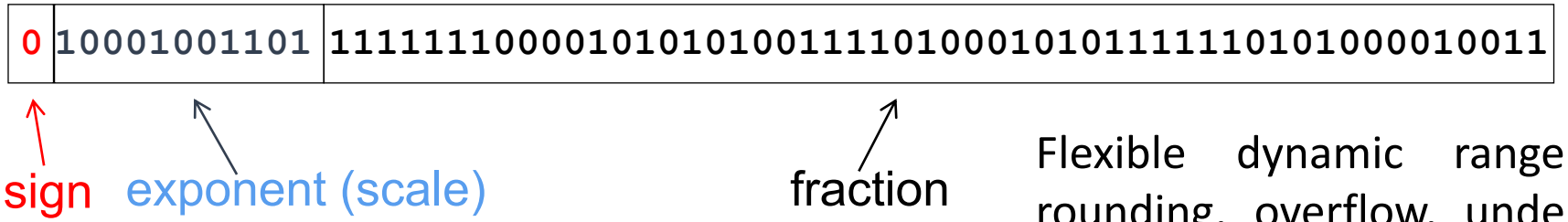

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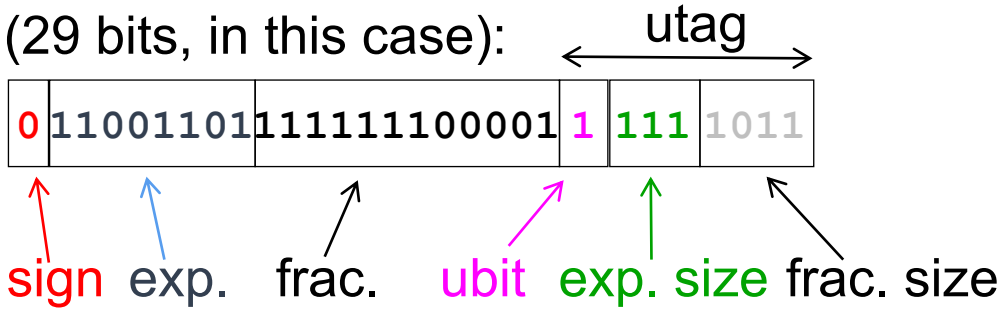


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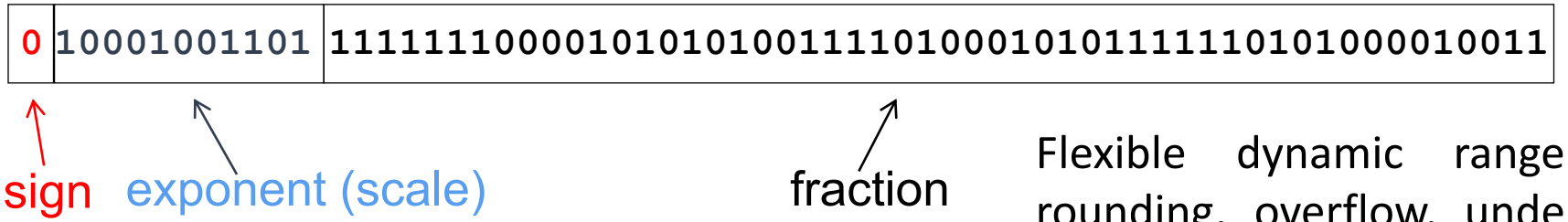

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Can unum ultimately become the future of computing?
We don't know yet…
Some known issues with unum:
- expensive in terms of time and power consumption
- Each computation in unum space is likely to change the bit length of the structure
- …

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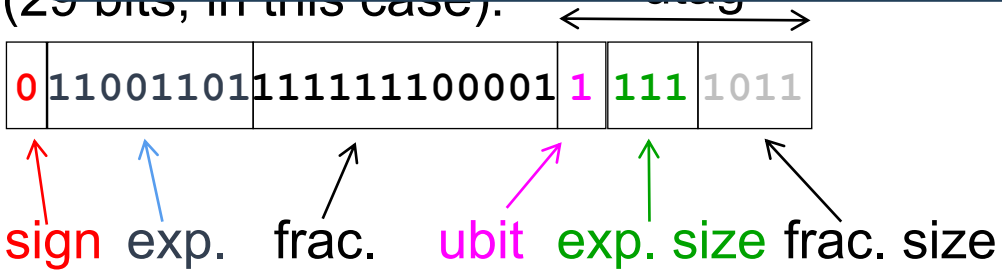


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