Hardware Fundamentals [CESE4005]

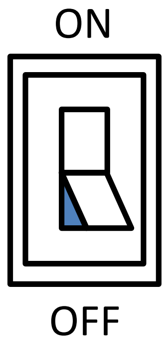
Lecture 1.1: Introduction to FET transistors, CMOS gates and semiconductors

September 2024

TU Delft

Transistor: The Building Block of Computers

- Microprocessors contain billions of transistors
  - Intel Broadwell-E5 (2016): 7 billion
  - IBM Power 9 (2017): 8 billion
  - Intel Ponte Vecchio (2021): 100 billion (is it a CPU?)
- Logically, each transistor acts as a **switch**
- Combined to implement **logic functions**
  - AND, OR, NOT, …



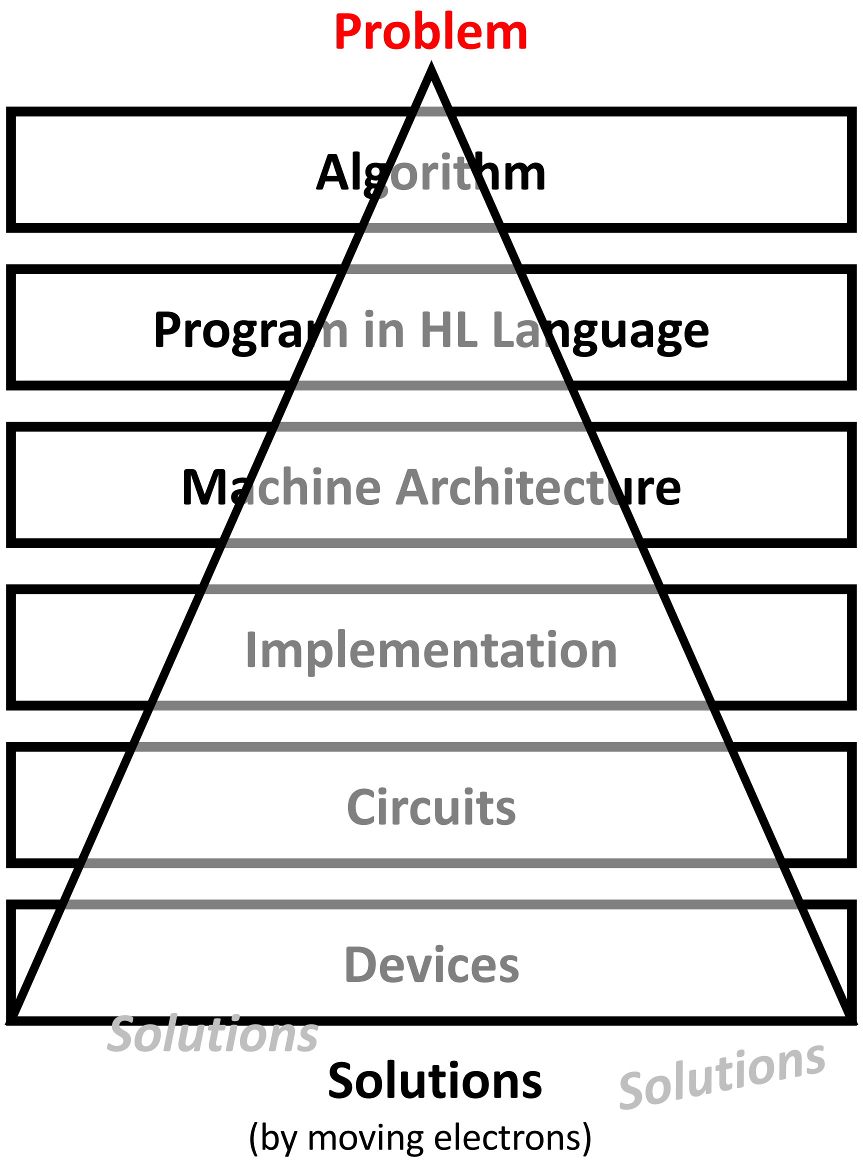
Combined to build **higher-level structures**

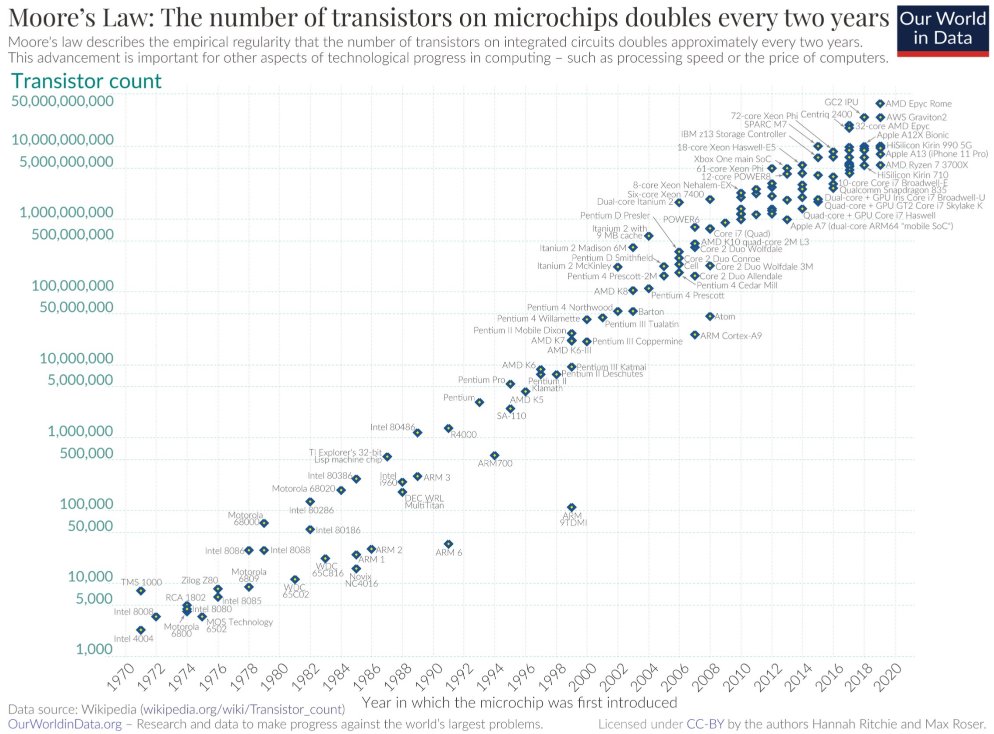
- Adder, multiplexer, decoder, register, …

Combined to build a **processor**

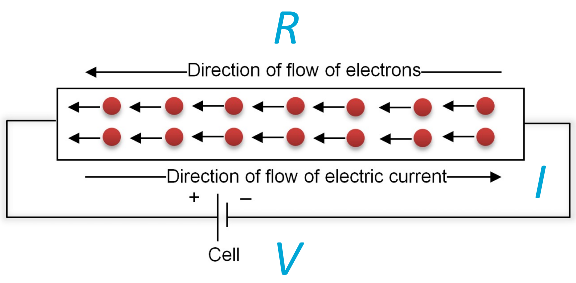
- RISC-V (but also LC-3)

Transistors position in the computing stack

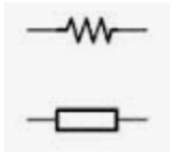




Very Basic Electrical Circuits Cheat Sheet

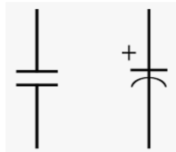


Resistor R



conductor

Capacitor C



insulator

?

Ohm's Law

$$I = \frac{V_T}{R}$$

Voltage Drop

$$V_x = I_x * R_x$$

Watt's Law

$$P = V_T * I$$

Current

$$I = \frac{q}{t}$$

$1\ C = 6.25 * 10^{18}$ *electrons*

Series circuits (sub-circuits)

$$I_T = I_1 = I_2 = I_3 = \ldots.$$

$$R_T = R_1 + R_2 + R_3 + \ldots.$$

$$I_T = \frac{V_T}{R_T}$$

KVL

$$V_T = V_1 + V_2 + V_3 + \ldots.$$

Voltage Division (for series resistors)

$$V_x = \frac{R_x}{R_T} * V_T$$

Power

$$P = V_T\, I = I^2\, R = \frac{V_T^2}{R}$$

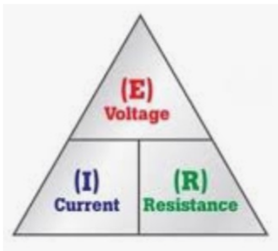
$$1\ hp = 746\ W$$

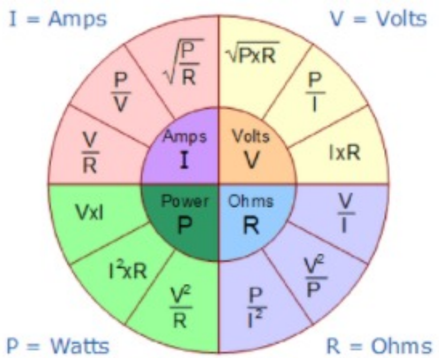
Energy

$$Energy = P\ t$$

$$Cost = Energy * \frac{cost}{kW{\cdot}h}$$

P in kW
t in h
Energy in kW•h





...

Parallel circuits (sub-circuits)

$$V_T = V_1 = V_2 = V_3 = \ldots.$$

$$\frac{1}{R_T} = \frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} + \ldots.$$

$$I_T = \frac{V_T}{R_T}$$

KCL

$$I_T = I_1 + I_2 + I_3 + \ldots.$$

Current Division (for parallel resistors)

$$I_x = \frac{R_{eq}}{R_x} * I_T$$

Current Division (for 2 parallel resistors)

$$I_x = \frac{Opposite}{Sum} * I_T$$

Two resistors in parallel

$$R_1 \parallel R_2 = \frac{R_1 * R_2}{(R_1 + R_2)}$$

n equal resistors in parallel

$$R_T = \frac{R}{n}$$

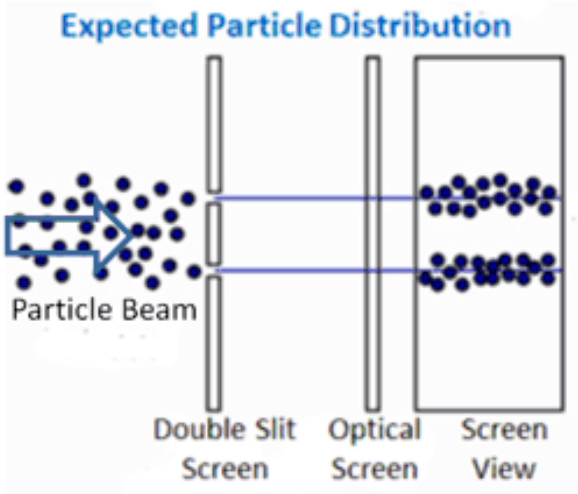
Conductance

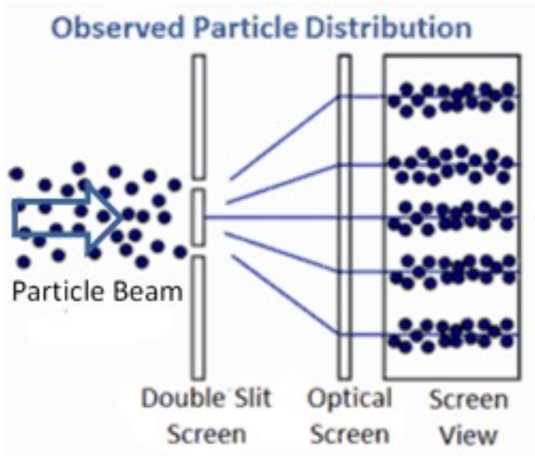
$$G = \frac{1}{R}$$

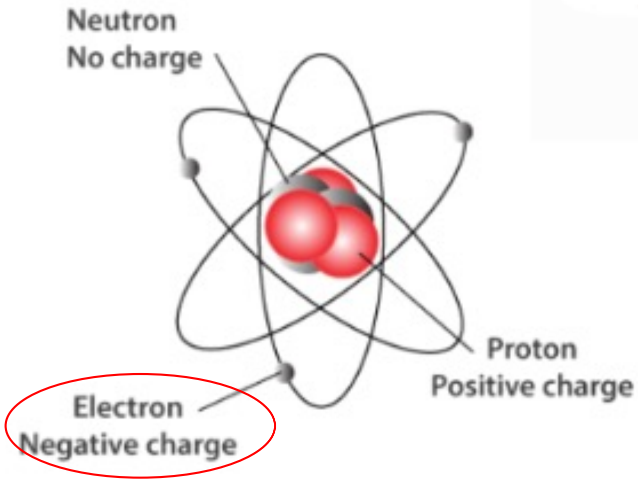
$$G_T = G_1 + G_2 + G_3 + \ldots.$$

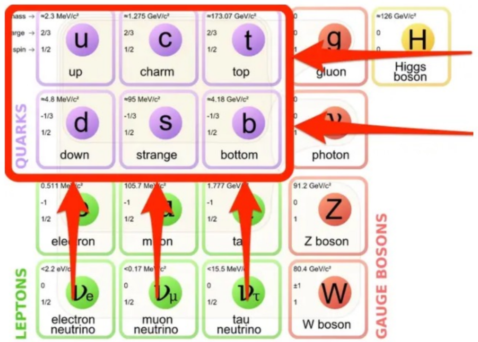
$$I_T = V_T\, G_T$$

Electrons must be important particles (however)









The Standard Model with the six quarks clearly indicated. MissMJ on Wikipedia

Physicists just discovered a different type of particle that will spawn an entirely new field of research

Jessica Orwig Jul 15, 2015, 11:05 PM CEST

A Simple Switch Circuit

- A wall switch determines whether current flows through the light bulb

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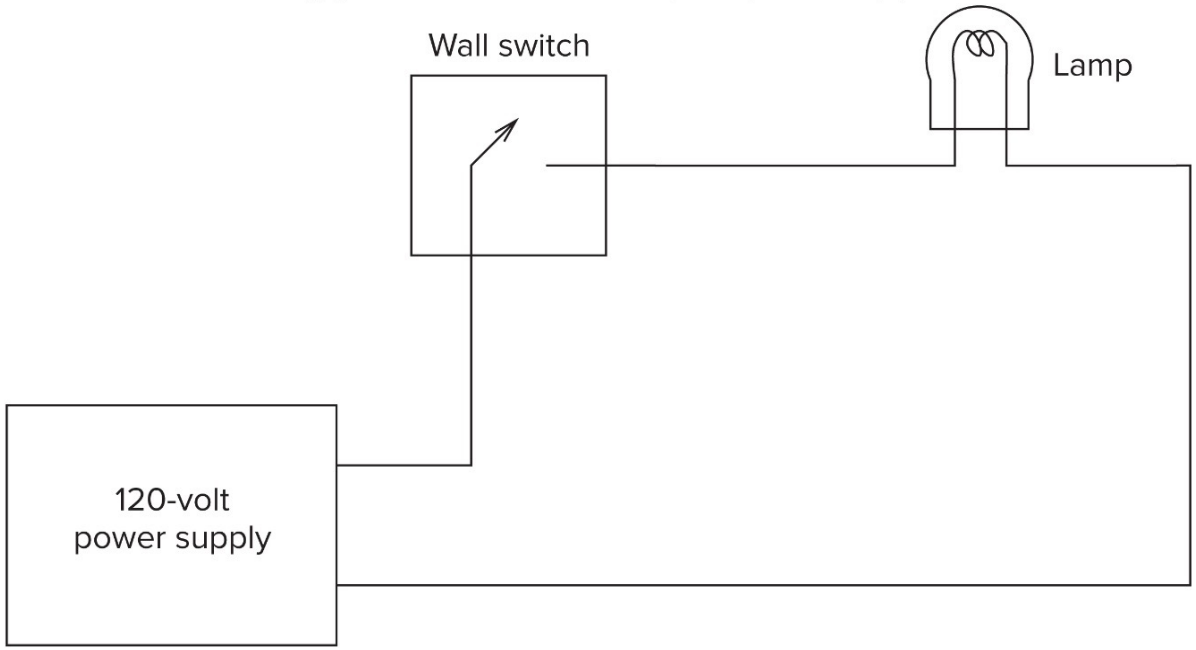

- If switch is closed, current flows, lamp is **ON**, voltage across lamp is **non-zero**
- If switch is open, no current flows, lamp is **OFF**, voltage across lamp is **zero**

Transistor = Voltage-Controlled Switch 1

- Figure shows an **N-type** transistor
  When Gate voltage is **positive**, relative to Source, transistor acts as a short circuit: a **closed** switch
- When Gate voltage is zero (or negative), relative to Source, transistor acts as an open circuit: an open switch

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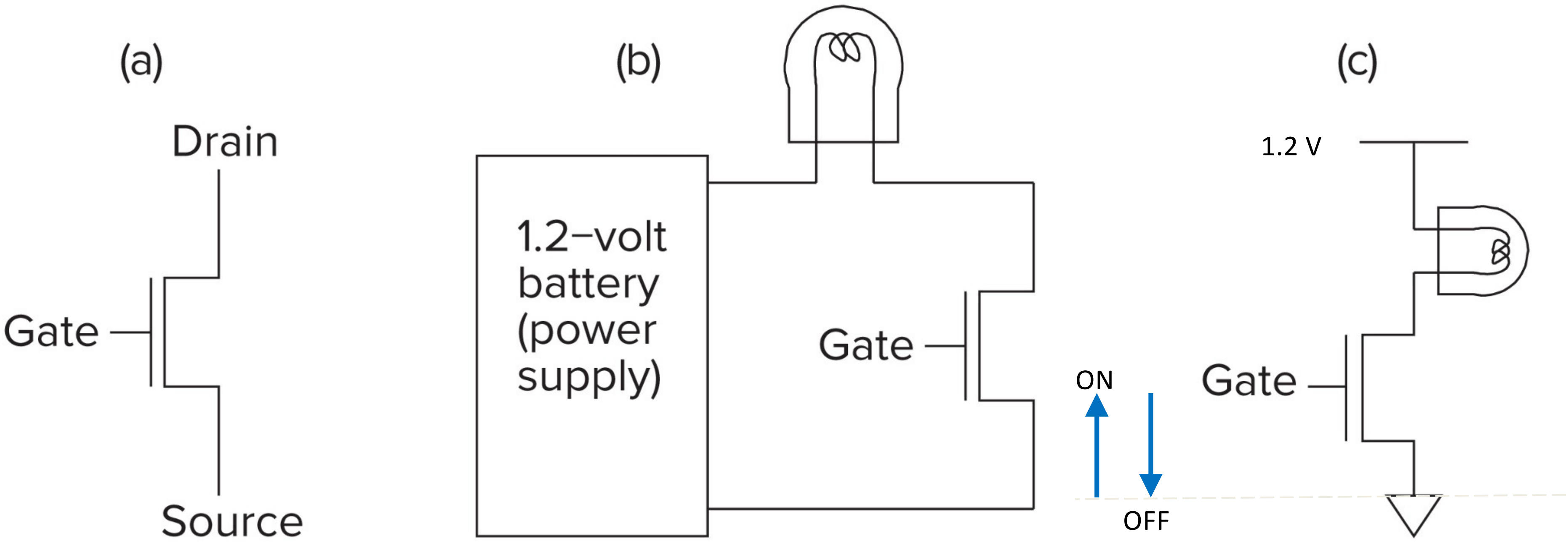

Transistor = Voltage-Controlled Switch 2

- Consider the circuit below. The bar at the top represents the high voltage rail (+1.2V) and the triangle at the bottom represents ground (0V)

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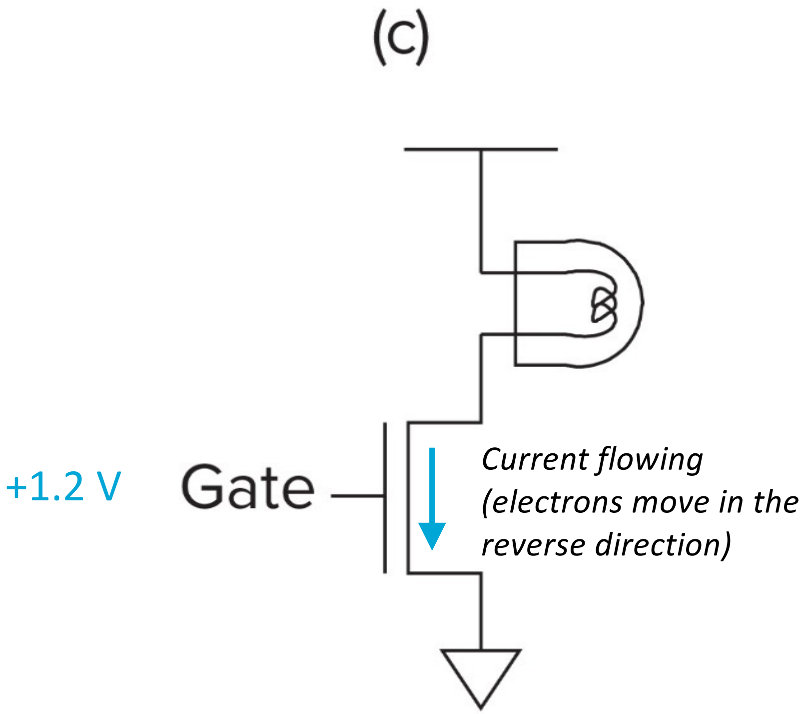

- **When Gate = +1.2V, what happens?**
  - Gate-to-source voltage > 0
  - Transistor = closed switch
  - Current flows, lamp is **ON**
- **When Gate = 0V, what happens?**
  - Gate-to-source voltage = 0
  - Transistor = open switch
  - No current flows, lamp is **OFF**

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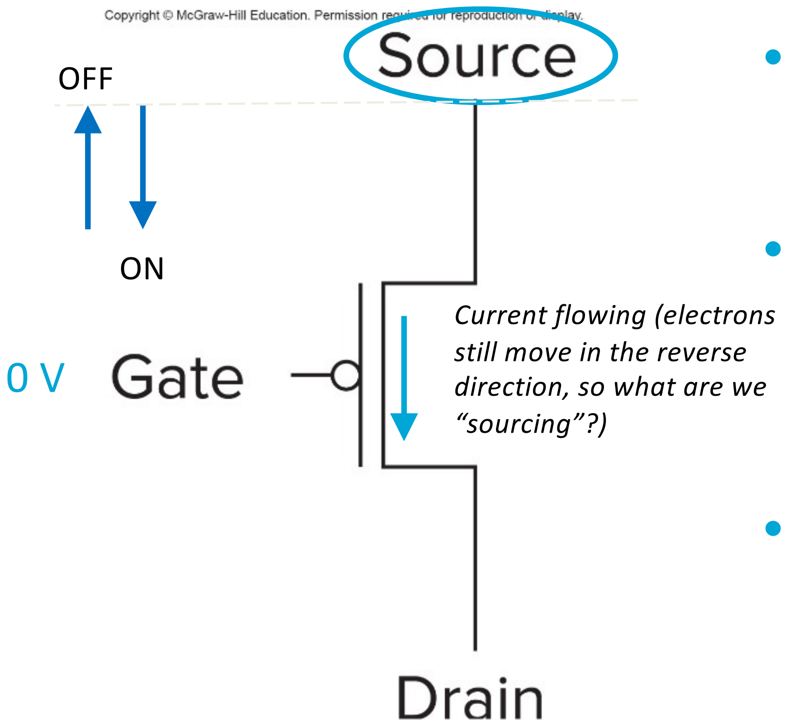
Transistor = Voltage-Controlled Switch 3

- A different type of transistor is shown below, the **P-type** transistor. Notice the little "bubble" on its gate

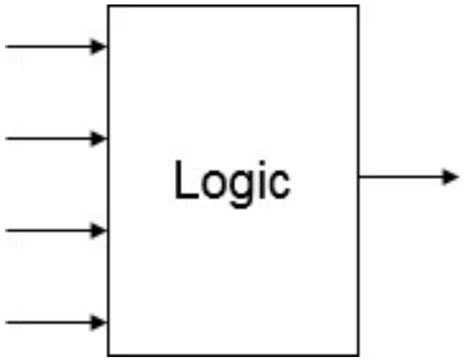


- When Gate voltage is **negative**, relative to Source, transistor acts as a short circuit: a **closed** switch
- When Gate voltage is zero (or positive), relative to Source, transistor acts as an open circuit: an open switch
- NOTE: This behavior is the opposite of the N-type. Behavior is complementary

- We use both N-type and P-type transistors together to implement logic gates. This is known as **CMOS** or Complementary MOS logic

Logic Gate

- A logic gate is a circuit that transforms binary input signals into a single binary output signal. Signals are the voltages.
- Binary: +1.2V = 1 (true), 0V = 0 (false)
  - P-type transistors: source connected to +1.2V
  - When gate = 1, transistor is OFF
  - When gate = 0, transistor is ON
  - N-type transistors: source connected to 0V
  - When gate = 1, transistor is ON
  - When gate = 0, transistor is OFF



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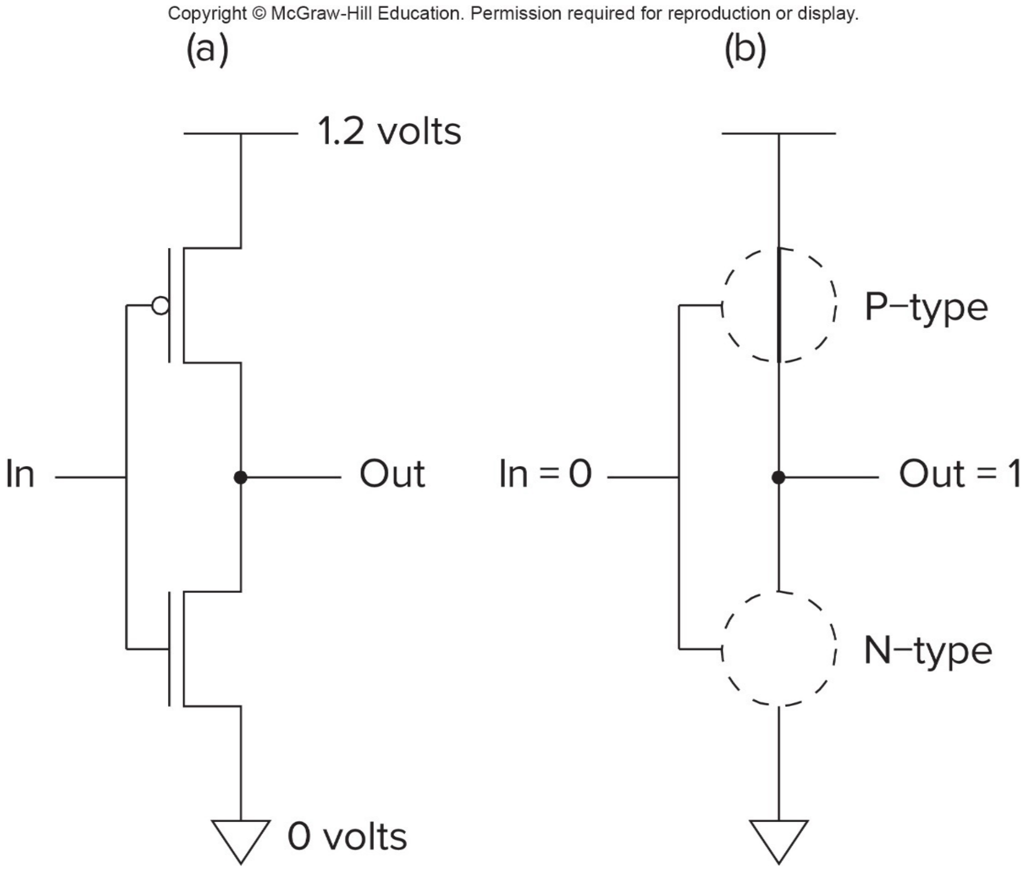
NOT Gate (Inverter)



- **Example:**
- When input = 0, P-type transistor turns on and N-type transistor turns off. Output is connected to +1.2V, so output = 1

- Logic gate is described using its **truth table**

Input	Output
0	1
1	0

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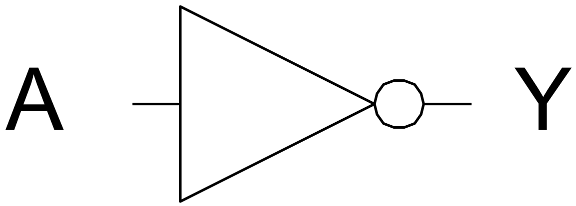
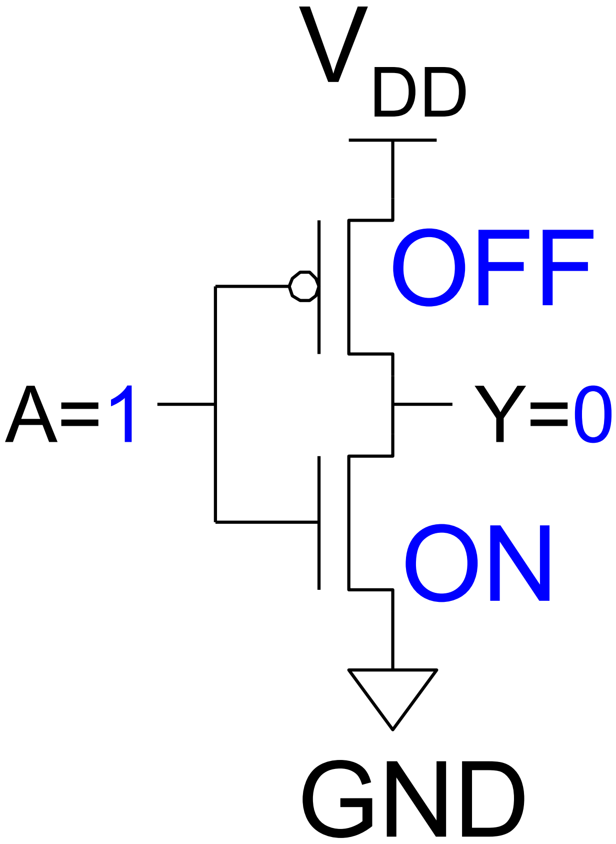
Inverter (animated)

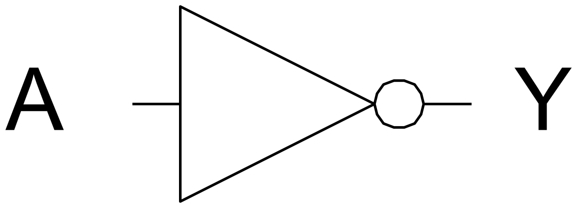
A	Y
0	
1	**0**

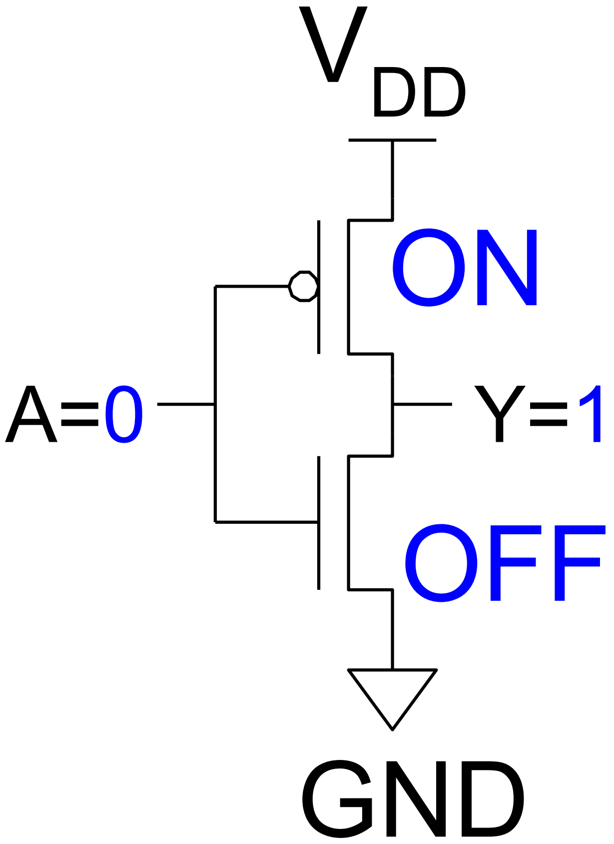




Inverter (animated)

A	Y
0	**1**
1	0





NOR Gate

- When either input is 1, output is 0

- **Example:**
- When B = 1, N-type transistor turns on and output (C) is connected to GND. Both inputs must be 0 to connect C to +1.2V.

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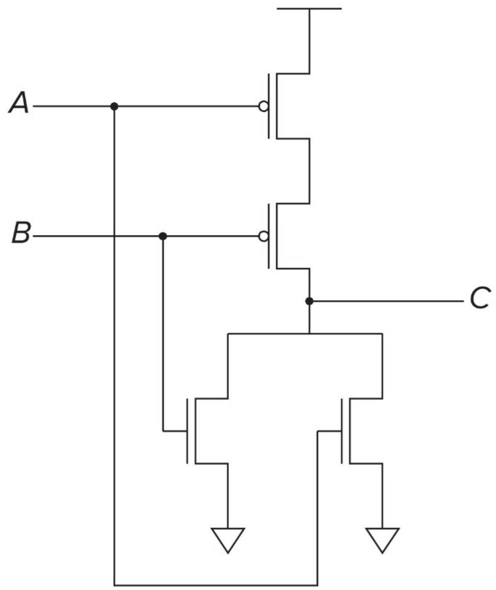
(a)



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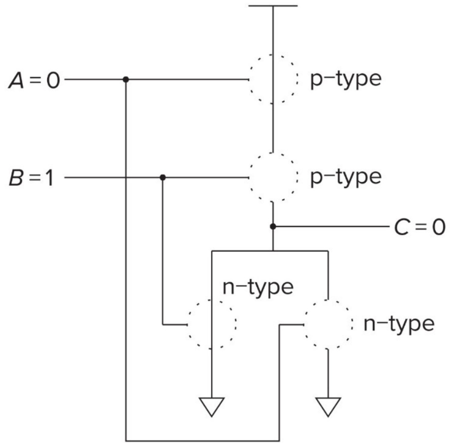
(b)



A	B	C
0	0	1
0	1	0
1	0	0
1	1	0

C = **N**OT(A **OR** B)

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The OR Gate

- When either input is 1, output is 1
  Add NOT after NOR

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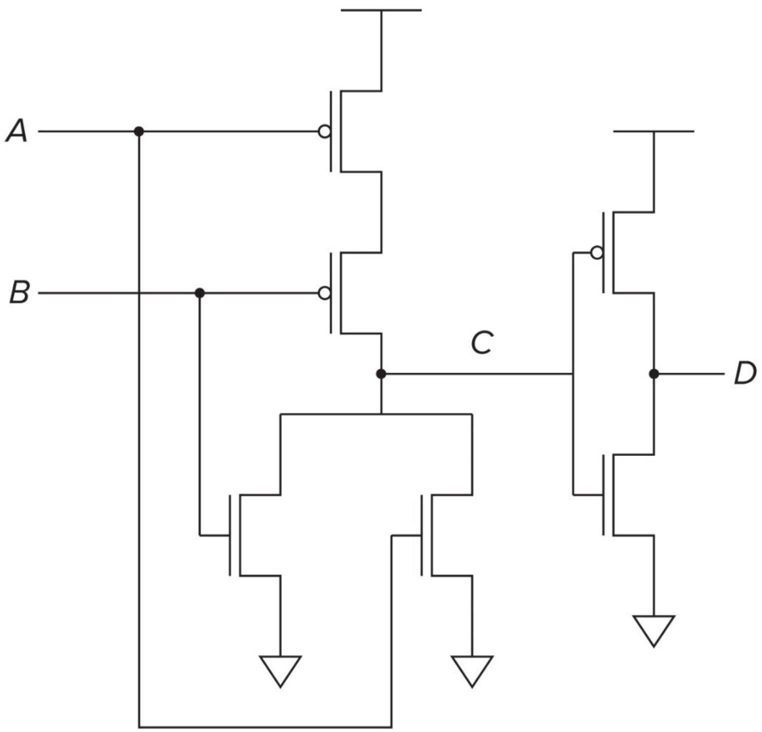
(a)



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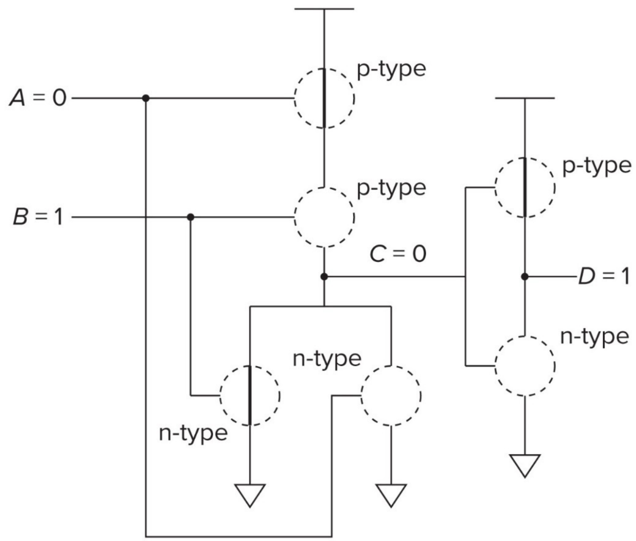
(b)



A	B	C	D
0	0	1	0
0	1	0	1
1	0	0	1
1	1	0	1

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Why do we need NOT after NOR?

- Why can't we simply put the P-type on the bottom and the N-type on top?

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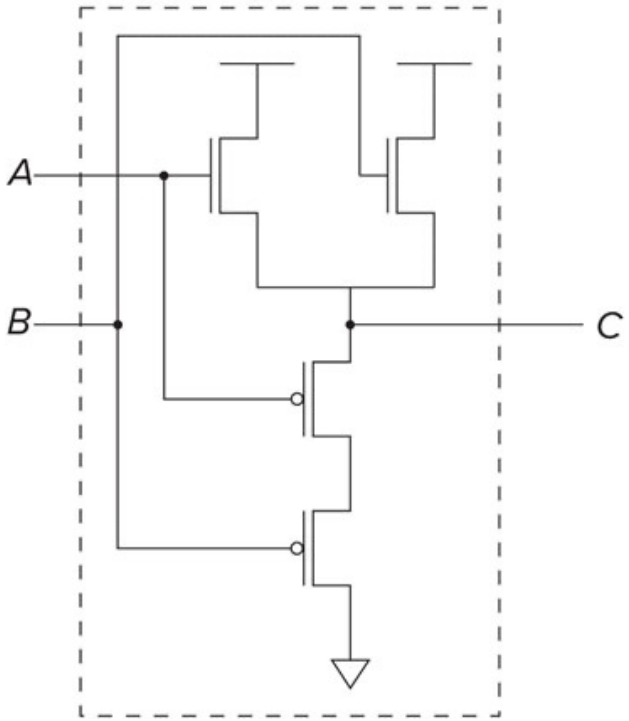
(a)



(b)

A	B	C
0 volts	0 volts	1.0 volts
0 volts	1.2 volts	0.7 volts
1.2 volts	0 volts	0.7 volts
1.2 volts	1.2 volts	0.7 volts

- *Does not work because of the electrical properties of the transistors.*
- Must **always** connect P to + and N to GND for CMOS circuit to work properly.

Maybe we should get to know more about transistors/electrons?

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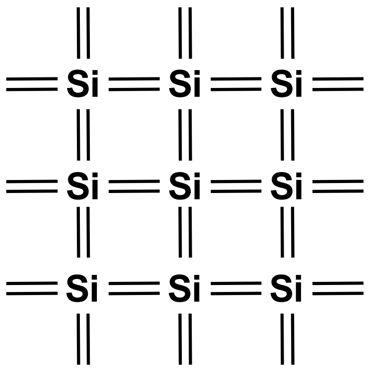
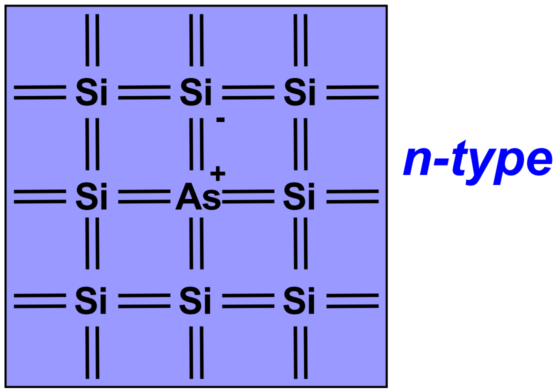
Semiconductor basics

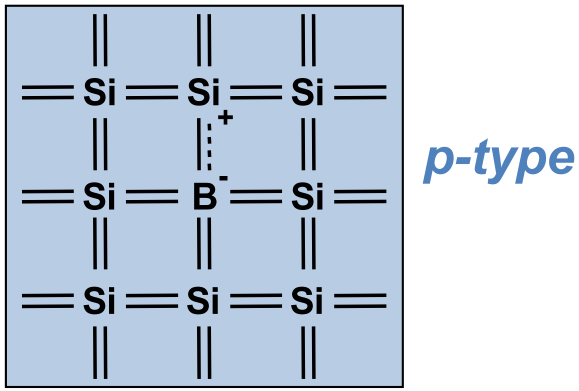
- Pure silicon (Si) is a very regular 3D-lattice (figure A)
- Conductivity is increased through *doping*, i.e. introducing impurities to this lattice (figures B and C)



Pure Si lattice

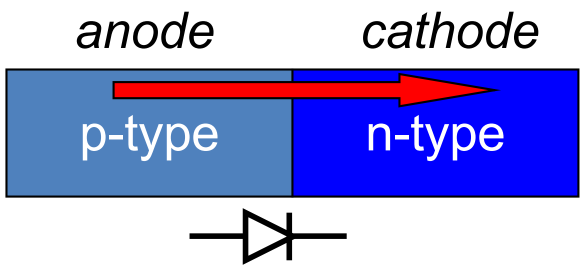


Group-V dopant (As^{+})

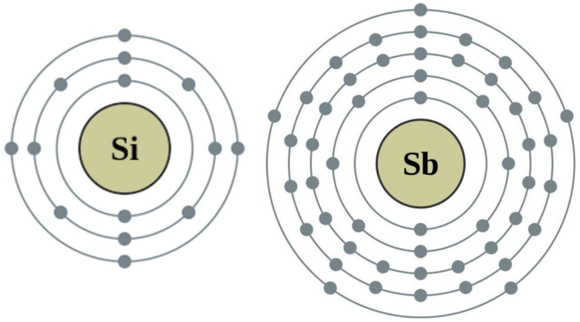


Group-III dopant (B^{-})

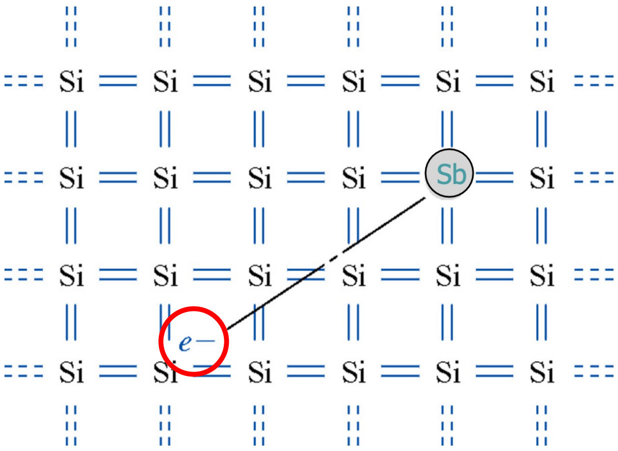
- **Extra** electrons: negative-charged, free carriers
- **Missing** electrons (“holes”): positive-charged, free carriers
- A pn-sandwich (“pn-junction”) effectively is a *diode*



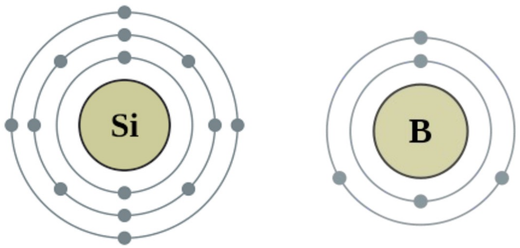
Semiconductor basics (more)



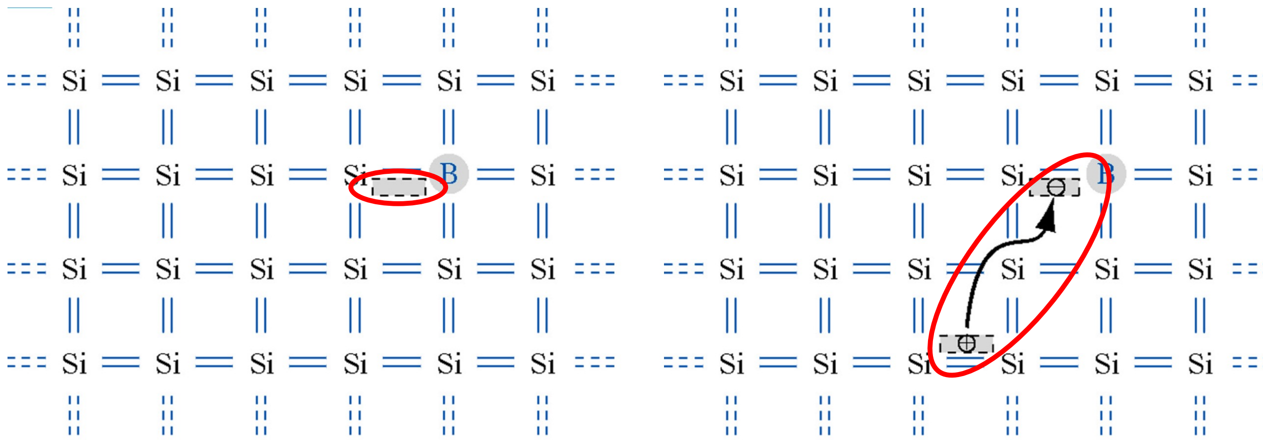
Silicon (Si) + Antimony (Sb)



The **donor** electron can become free with very small amount of thermal energy. (n-type)



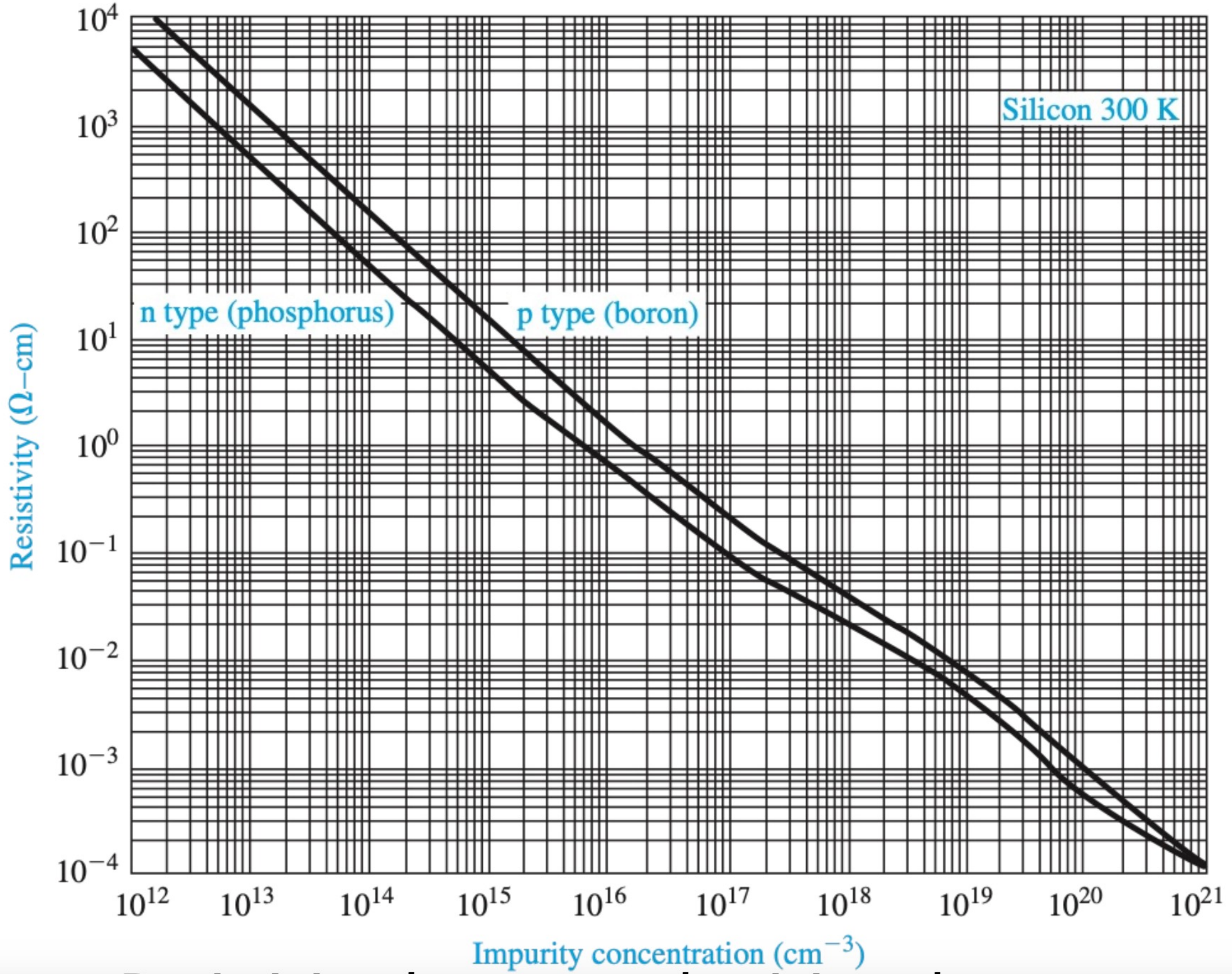
Silicon (Si) + Boron (B)

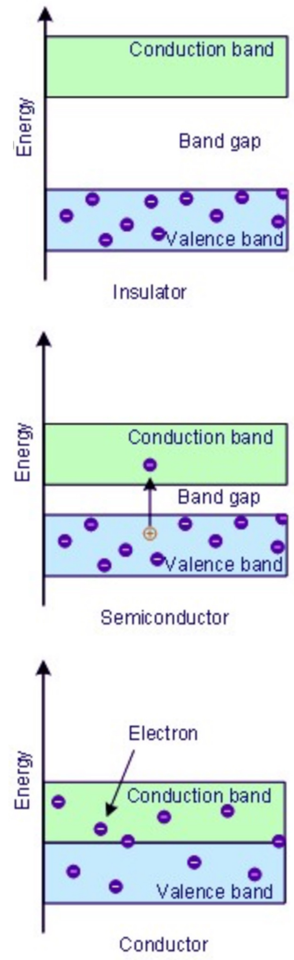


The **acceptor** has only three covalent electrons leaving one bound incomplete. With little thermal energy, valence electron breaks from a covalent bond and occupies this position (creating a hole). (p-type)

Q: which of the two conducts better?

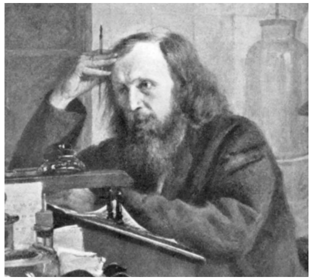
Semiconductor basics (conductance)



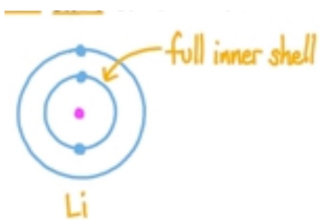


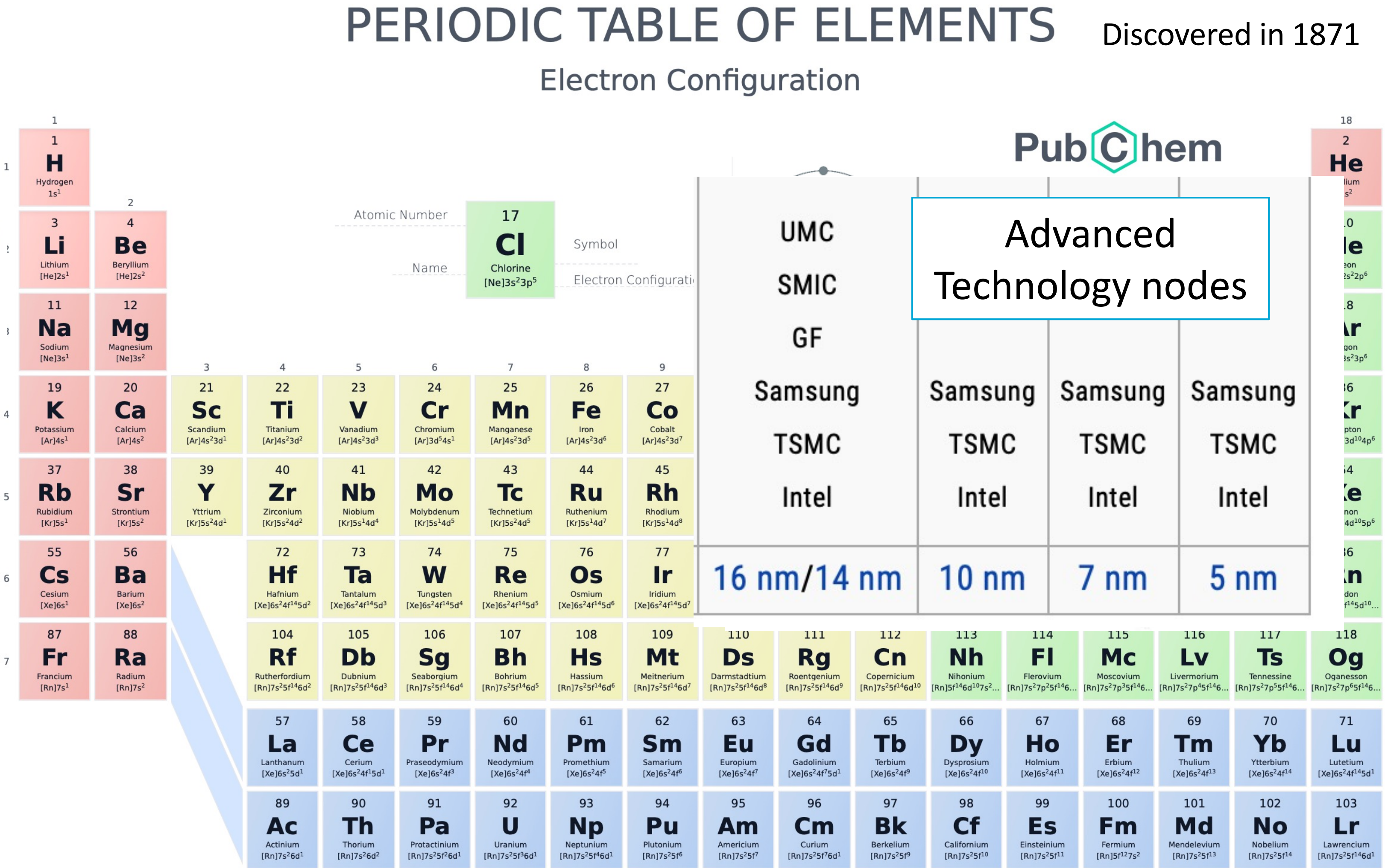
Resistivity, hence conductivity, changes over many orders of magnitudes; silicon is called **semiconductor**

Semiconductor basics (cont)



Discovered in 1871



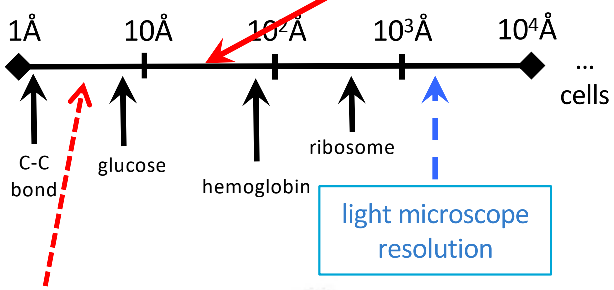


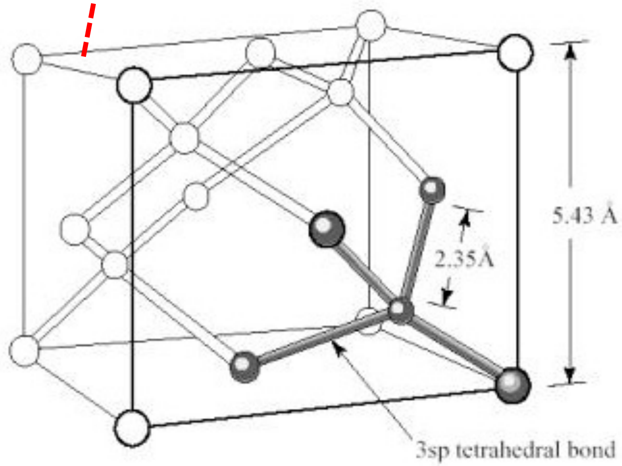
	Advanced Technology nodes		
UMC SMIC GF Samsung TSMC Intel	Samsung TSMC Intel	Samsung TSMC Intel	Samsung TSMC Intel
16 nm/14 nm	10 nm	7 nm	5 nm

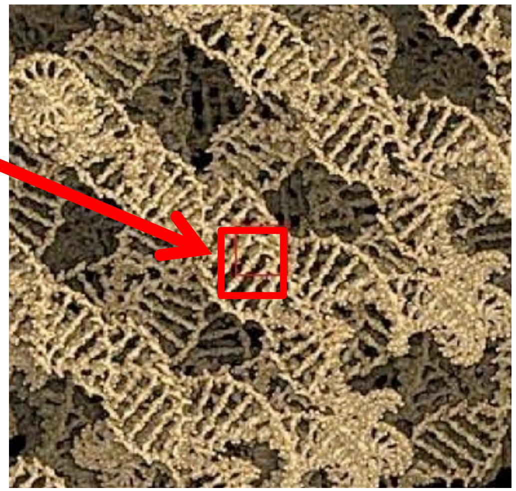
Think Ångströms not nanometers

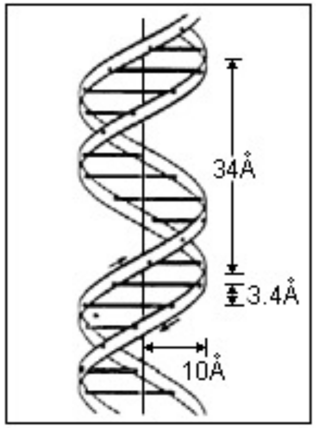
We should steer the movements of almost each individual electron to solve our specific problem

0.1 nm → 1 Å
5 nm → **50 Å**



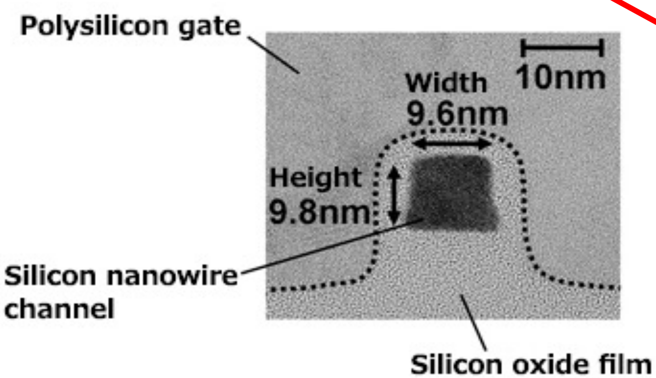


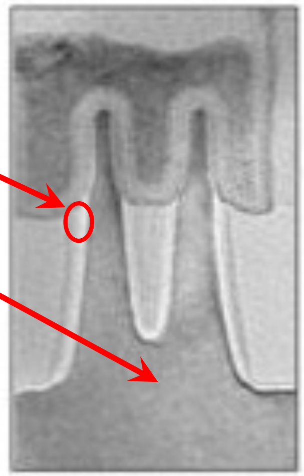

DNA



Very few atoms!
(e.g., 3nm / 30Å → **6 to 12 atoms**)

100s of Si atoms in 14nm



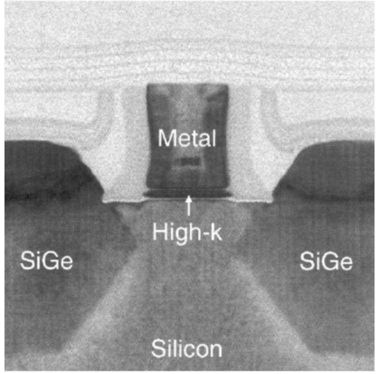

14 nm Process

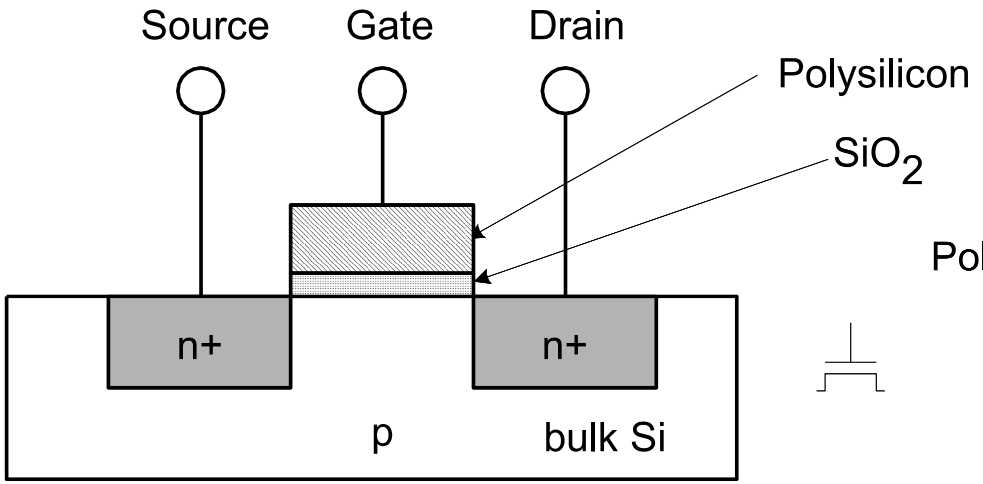
Ongoing transistor device advancements

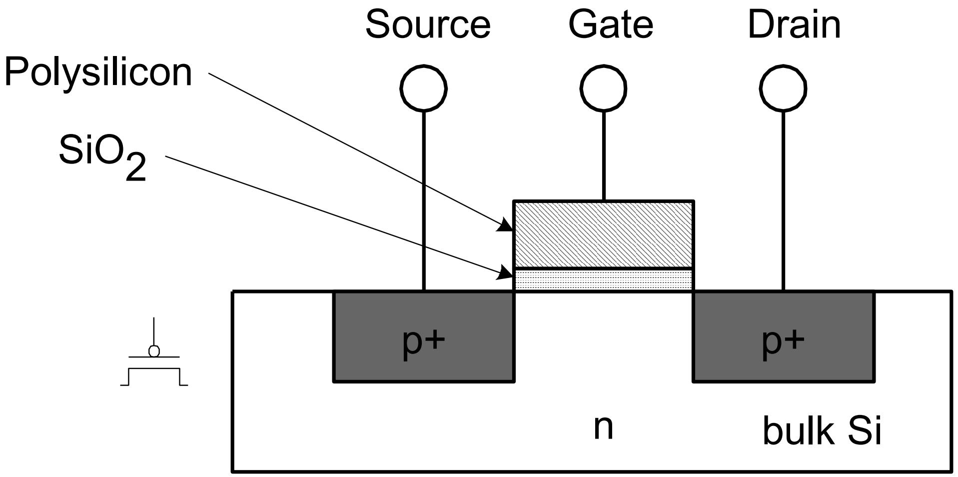
Qingzhu Zhang, Yongkui Zhang, Yanna Luo, Huaxiang Yin, *New structure transistors for advanced technology node CMOS ICs*, National Science Review, Volume 11, Issue 3, March 2024, nwae008, https://doi.org/10.1093/nsr/nwae008

The MOS FET transistor

- MOS FET (**M**etal-**O**xide **S**emiconductor **F**ield-**E**ffect **T**ransistor): a sandwich structure of p-type Si, n-type Si and insulator (SiO_2) materials
- It comes in two flavors: **nMOS** and **pMOS**:







Next Time

We continue …

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