CESE4005: Hardware Fundamentals

2024-2025, lecture 4

Introduction to Verilog: Part 1

Computer Engineering Lab

Faculty of Electrical Engineering, Mathematics & Computer Science

2024-2025

Anteneh Gebregiorgis

TU Delft

Delft University of Technology

Objectives

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- Be able to understand Verilog HDL description
- Be able to write a simple Verilog HDL description using a limited set of syntax and semantics
- Understanding the need for a “hardware view” when reading and writing an HDL

Overview

- HDL introduction
- Verilog basics and syntax
- Modules
- Assignments
- Initial and always blocks
- Structural modeling
- Dangers of Verilog
- Delays
- Testbenches

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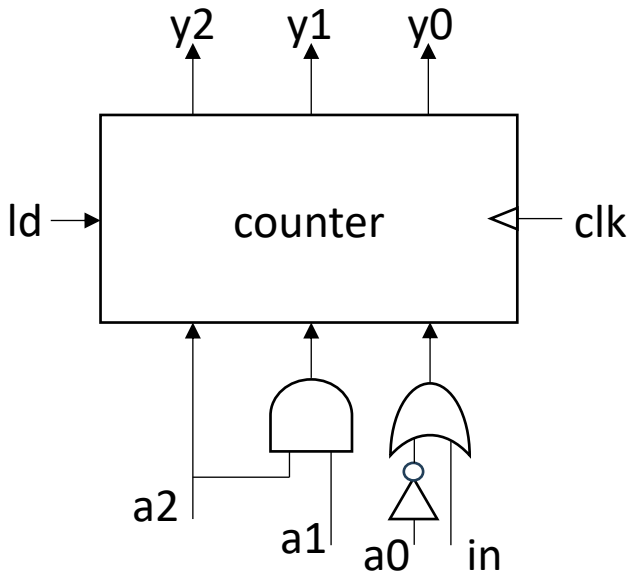


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        input clk, ld, a2, a1, a0, in,
        output y2, y1, y0);

   wire n1, n0, ninv;

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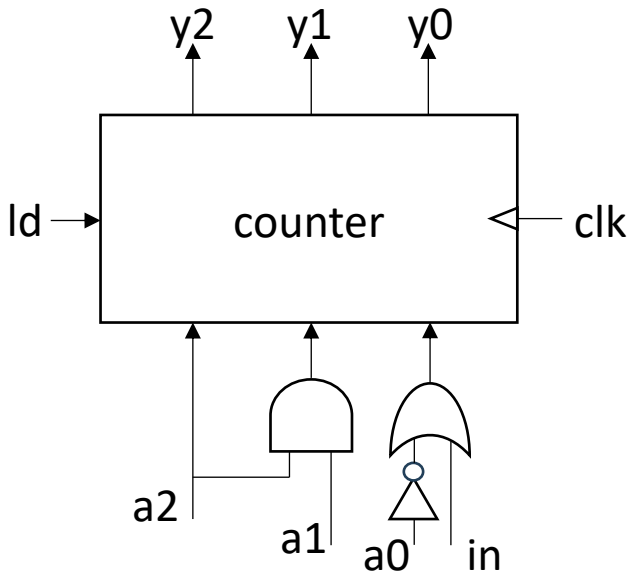


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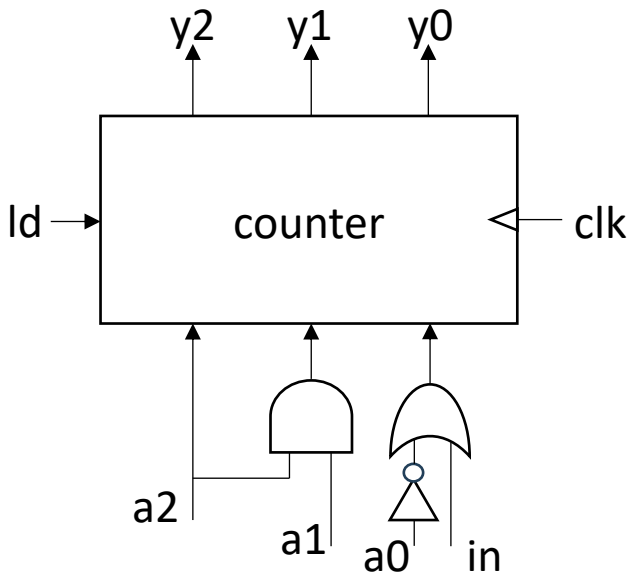


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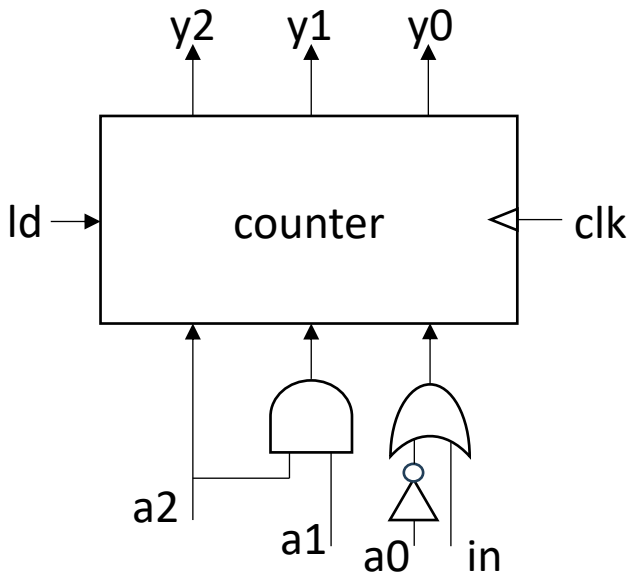
  - VHDL is more verbose and cumbersome

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- **Synthesis**
  - Logic synthesizer transforms HDL code into a *netlist* describing the hardware (i.e., a list of gates and the wires connecting them)
  - Optimization is performed to reduce the amount of hardware.
  - The output netlist maybe a Verilog file, or a schematic to visualize the circuit.

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IMPORTANT:

When using an HDL, think of the **hardware** the HDL should produce, then write the appropriate idiom that implies that hardware.

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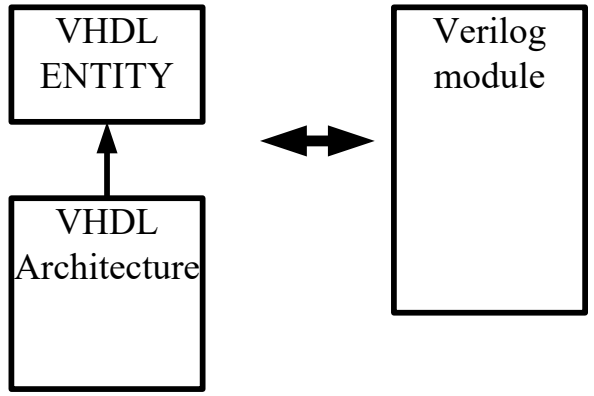

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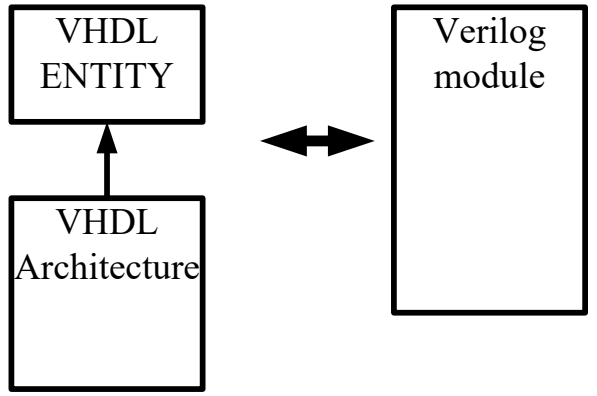

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- **SystemVerilog ➔ based on Verilog with more features**
  - it is like C++ of Verilog
  - More datatypes & feature
  - Easy to learn/switch to from Verilog

Verilog basics and syntax

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- **Comments: // single line comment**
  - **/* multiline**

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Another way of grouping operators

Operator types	examples
Bitwise	~, &, |, ^, ^~
Arithmetic	+, -, *, /, %, >>, <<
Relational/equality	>, <, >=, <=/ ==, !=
logical	&&, ||, !

Operator precedence

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~	NOT
*, /, %	mult, div, mod
+, -	add, sub
<<, >>	shift
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E.g., `~a & b + c` is evaluated as `(~a) & (b + c)`

Verilog lexical conventions

Concatenation & Replication Operators

{id_1, id_2, …} ➔ Concatenates id_2 at the end of id_1

{n{id}} ➔ replicates id *n* times

- Examples: assign conc_reg = {REG_IN[6:0],Serial_in},

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    - *4'b1111 ➔ 4-bit binary number*
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    - *'o7460 ➔ is an octal number*
- *String values ➔ any value within " "*

Numbers

Format: N'Bvalue

N = number of bits, **B** = base

N'B is optional but recommended (default is decimal)

Number	# Bits	Base	Decimal Equivalent	Stored
3'b101	3	binary	5	101
'b11	unsized	binary	3	00…0011
8'b11	8	binary	3	00000011
8'b10101011	8	binary	171	10101011
3'd6	3	decimal	6	110
6'o42	6	octal	34	100010

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42	unsized	decimal (default)	42	00…0101010

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- Some net data types are ***wire, tri, wor, trior, wand, triand, tri0, tri1, supply0, supply1,*** and ***trireg***

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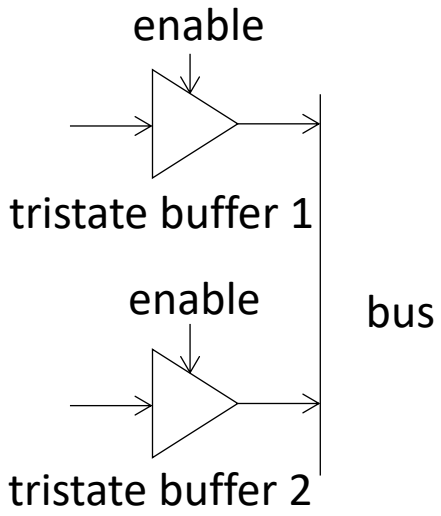
  - It is declared as an input or in-out port
  - On a left hand of a continuous assignment
- Some net data types are ***wire, tri, wor, trior, wand, triand, tri0, tri1, supply0, supply1,*** and ***trireg***
- Default value of net is ‘Z’ (except the “trireg” net, which defaults to x)

Z's and X's

- HDLs use z to indicate a floating value (not connected to a source).
- Similarly, HDLs use x to indicate an invalid logic level (or unknown/uninitialized value).
- z is particularly useful to describe a tristate buffer, whose output floats when the enable is 0.
- If a bus is simultaneously driven to 0 and 1 by two enabled tristate buffers (or other gates), the result is x, indicating contention.
- If all of the tristate buffers driving a bus are simultaneously OFF, the bus will float, indicated by z.



Resulting value of bus as a function of the buffer outputs

buffer 1 →

↓ buffer 2

	z	0	1
z	z	0	1
0	0	0	X
1	1	X	1

Data types: Registers

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- They retain the value until another value is placed to them
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- Verilog register do not need clock as hardware registers do

Data types: Vectors and Strings

- **Vectors**
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  - The width of the reg variable has to be large enough to hold the string
    - If the variable's size is smaller than the string, then Verilog truncates the leftmost bits of the string
    - If the variable's size is larger than the string, then Verilog adds zeros to the left of the string

Verilog modules

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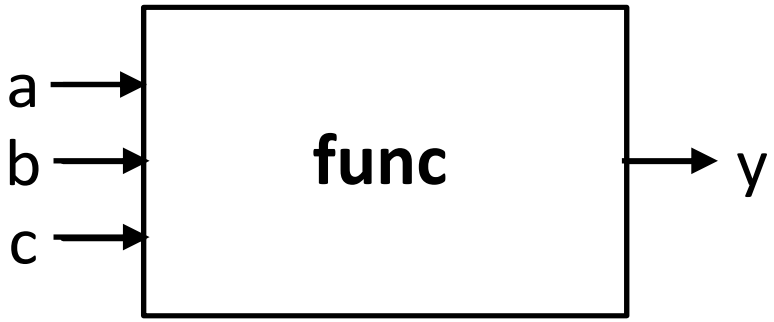
Example

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module func(input a, b, c,
            output y);

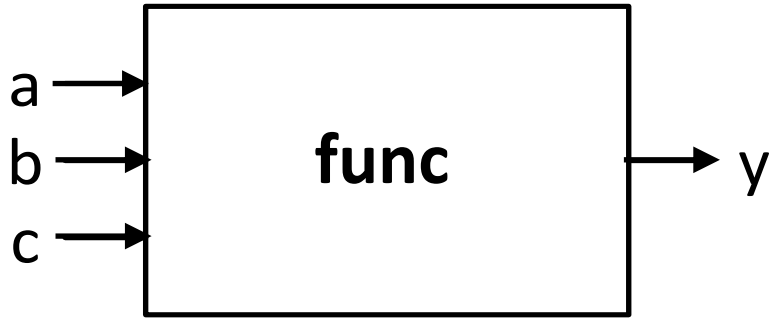
  // description of contents

endmodule
```

Verilog modules

- A module is the basic building block in Verilog
- Interfaces with outside using ***ports***
- Module can be an element or collection of lower-level design blocks
- Module cannot be nested

Example

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Verilog modules

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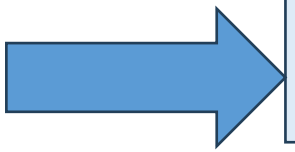

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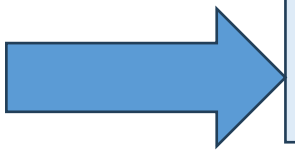

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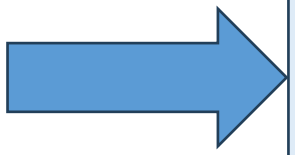

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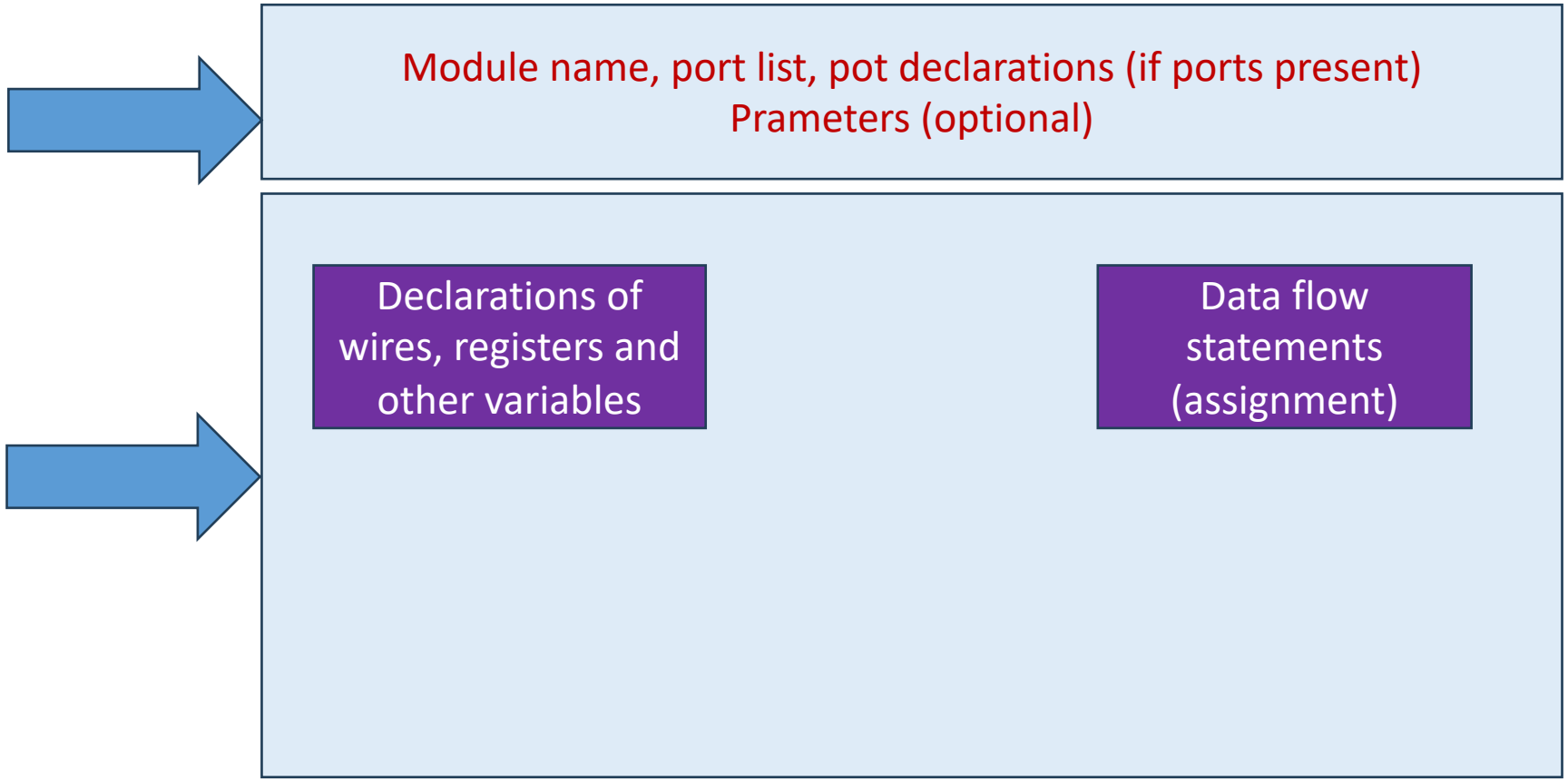

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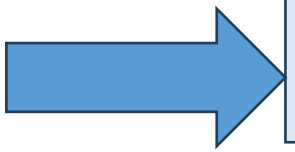

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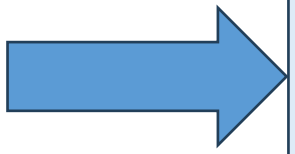

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module func1(input [3:0] a,    // creates a[3], a[2], a[1] and a[0]
             input b,
             output y);

   wire [3:0] k;  // creates k[3], k[2], k[1] and k[0]
   wire n;

   assign k = ~a;  // implies k[3] = ~a[3], k[2] = ~a[2] etc.
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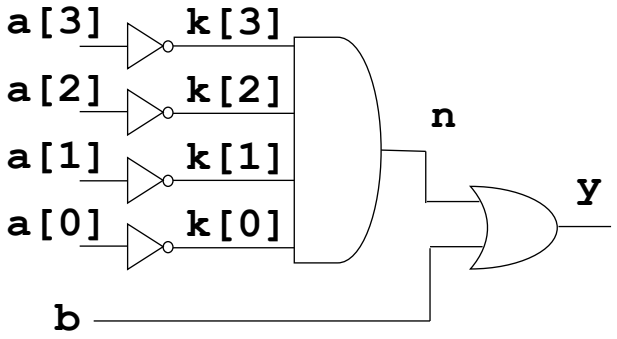
Equivalent circuit



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  inv  i2 (n1, n2);
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endmodule
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and3 and **inv** are other modules that are described elsewhere

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module gates(input [3:0]  a, b,
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   /* Five different two-input logic
      gates acting on 4 bit busses */
   assign y1 = a & b;    // AND
   assign y2 = a | b;    // OR
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   assign y4 = ~(a & b); // NAND
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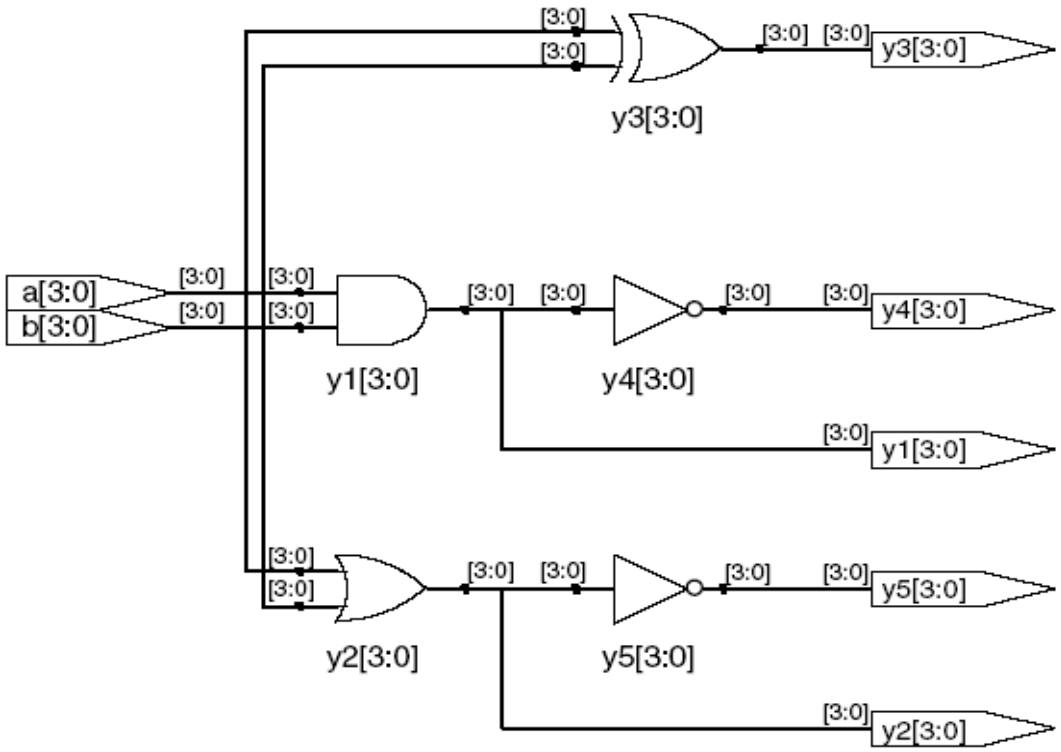

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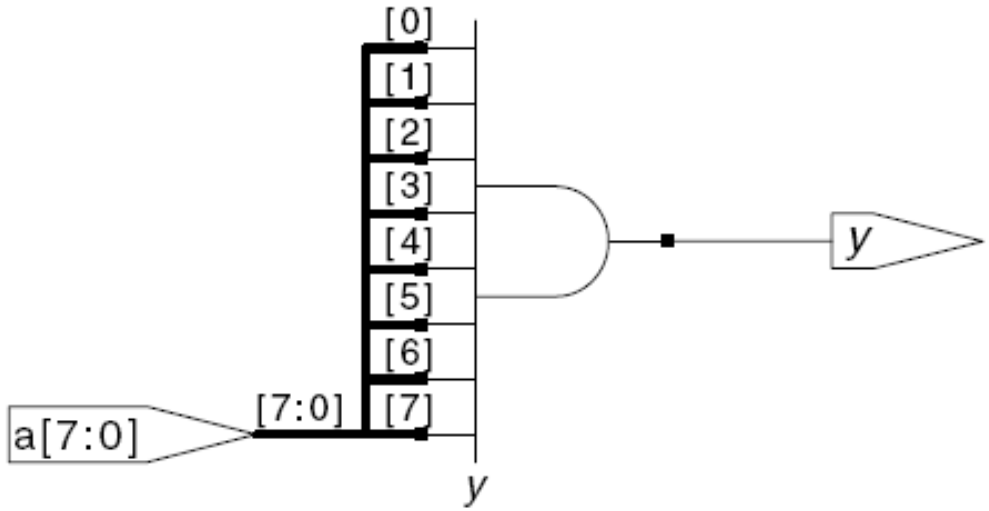

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   assign y = s ? d1 : d0;

endmodule
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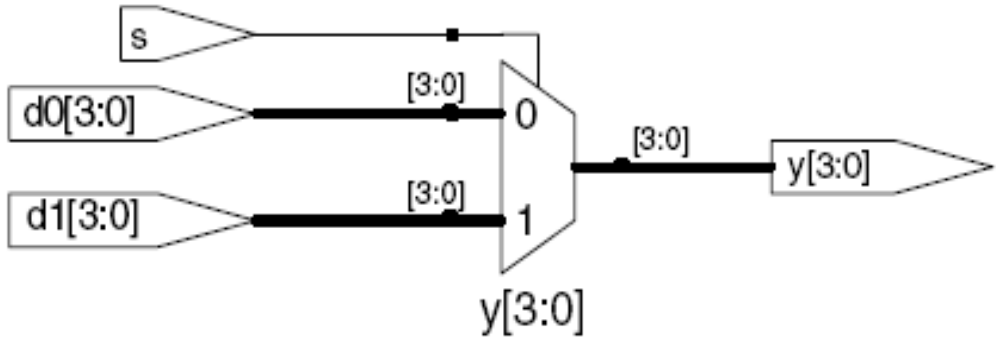

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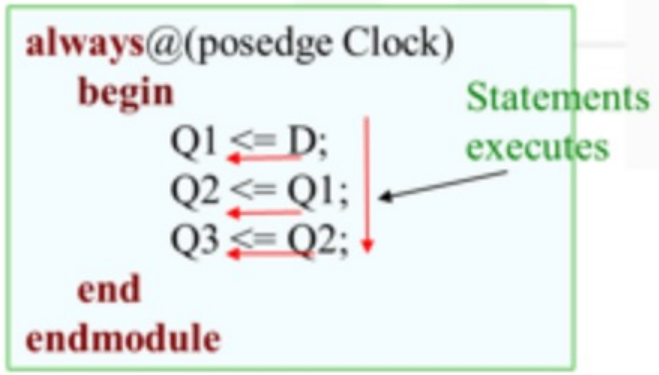

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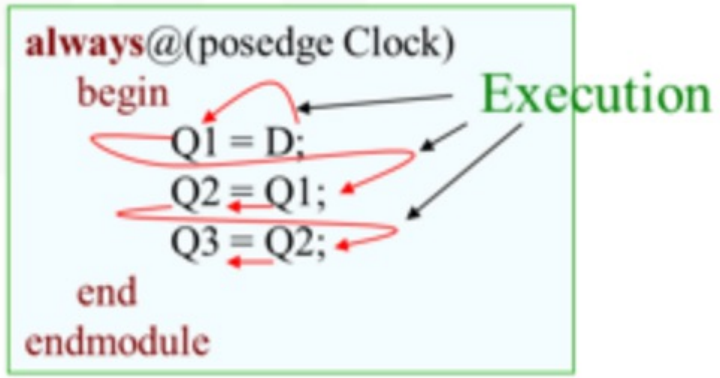

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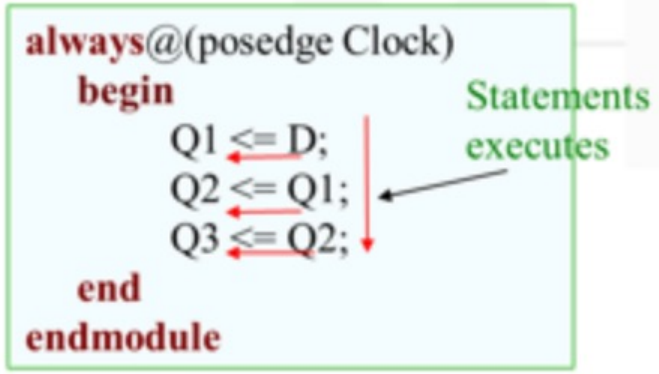

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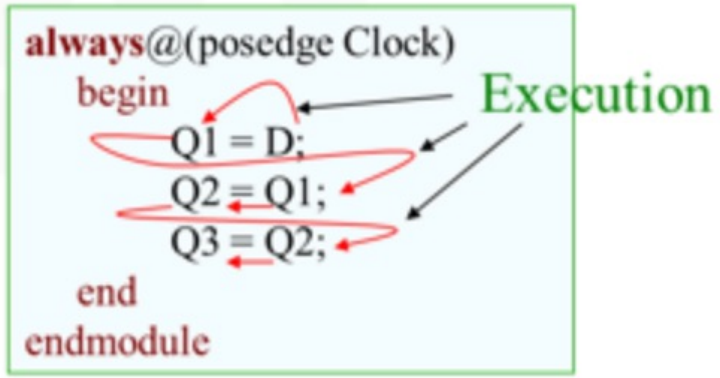

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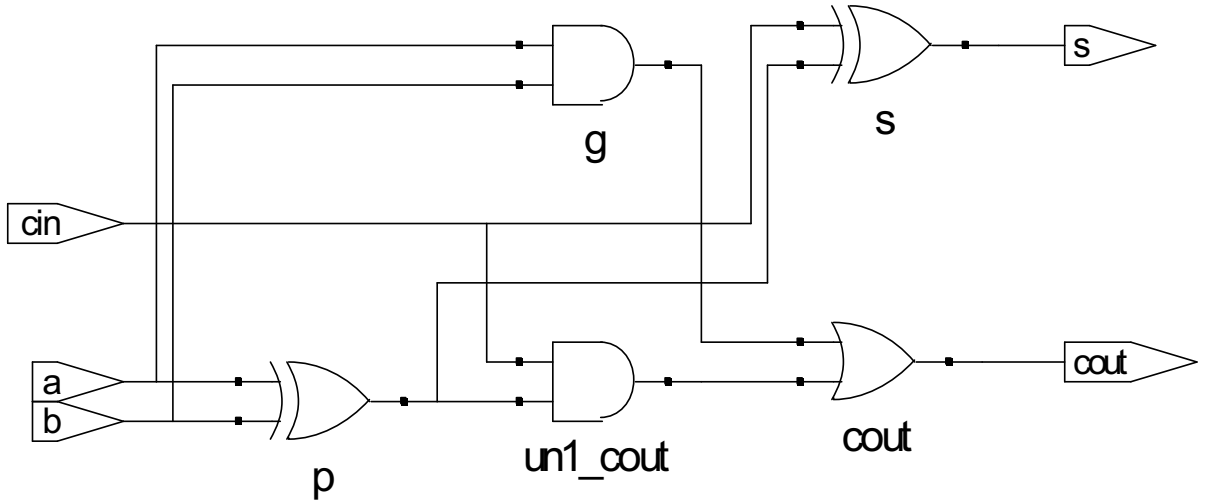

During synthesis, additional internal nodes (e.g. un1_cout) may be created

Z's and X's

```
module tristate(input [3:0] a,
                input en,
                output tri   [3:0] y);
   assign y = en ? a : 4'bz;
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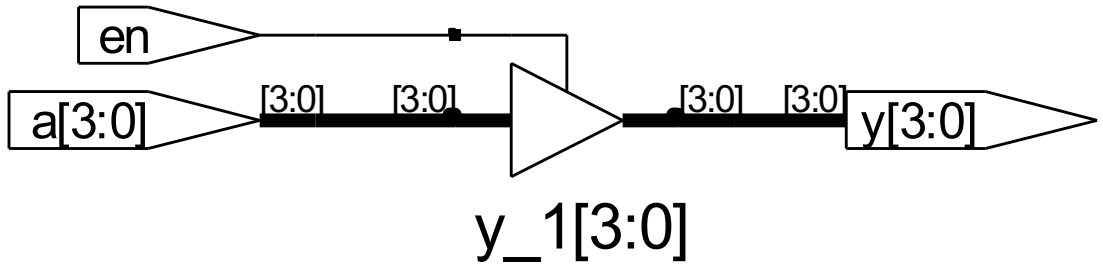

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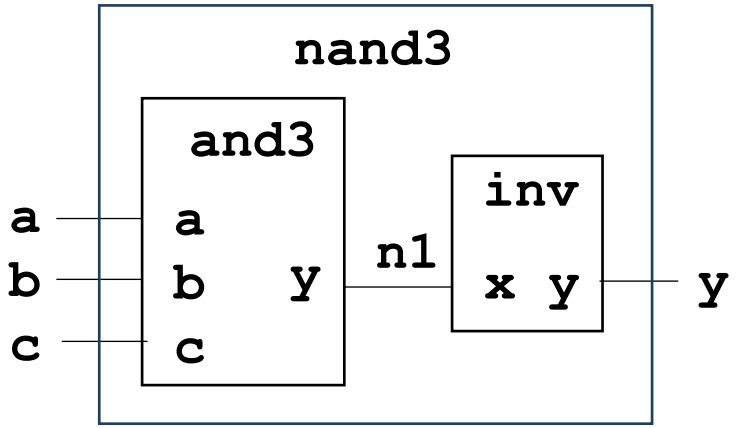

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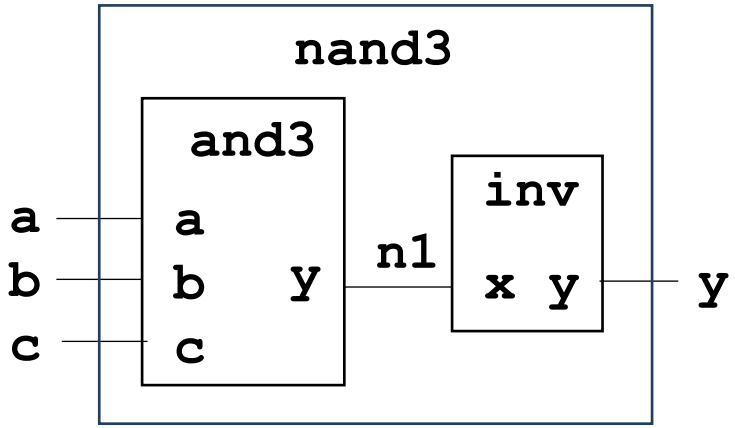
Example

```
module and3(input a, b, c,
            output y);
  assign y = a & b & c;
endmodule
```



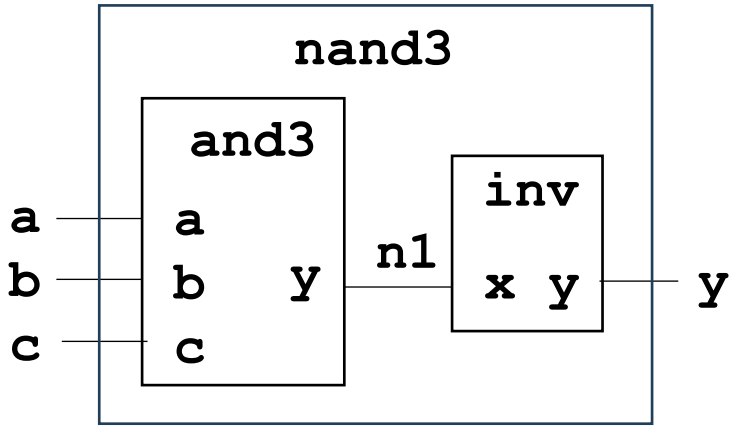
Structural Verilog

- The previous sections discussed behavioral modeling: describing a module in terms of the relationships between inputs and outputs.
- This section examines structural modeling: describing a module in terms of how it is composed of simpler modules.
- At the lowest level (leaf modules) you always need to use behavioral modelling.

Example

```
module and3(input a, b, c,
            output y);
  assign y = a & b & c;
endmodule

module inv(input x,
           output y);
  assign y = ~x;
endmodule
```



Structural Verilog

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- At the lowest level (leaf modules) you always need to use behavioral modelling.

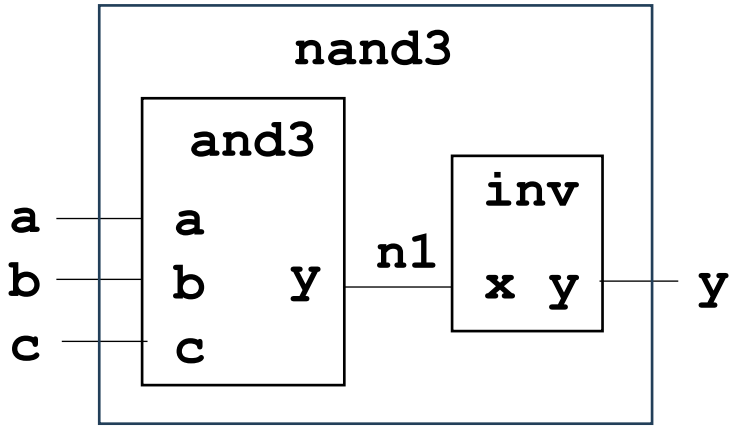
Example

```
module and3(input a, b, c,
            output y);
  assign y = a & b & c;
endmodule

module inv(input x,
           output y);
  assign y = ~x;
endmodule

module nand3(input a, b, c,
             output y);
  wire n1, n2;                    // internal signal

  and3 i1(a, b, c, n1);  // instance of and3
  inv  i2(n1, n2);        // instance of inv
  assign y2 = n2
endmodule
```



Structural Verilog

- Alternative specification of port connections

Structural Verilog

- Alternative specification of port connections

```
module and3(input a, b, c,
            output y);
  assign y = a & b & c;
endmodule

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           output y);
  assign y = ~x;
endmodule
```

Structural Verilog

- Alternative specification of port connections

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module and3(input a, b, c,
            output y);
  assign y = a & b & c;
endmodule

module inv(input x,
           output y);
  assign y = ~x;
endmodule

module nand3(input a, b, c,
             output y);
  wire n1;

  and3 i1(.a(a), .b(b), .c(c), .y(n1));
  inv  i2(.x(n1), .y(y));
endmodule
```

Structural modelling: 4:1 multiplexer

```
module mux4(input [3:0] d0, d1, d2, d3,
            input [1:0] s,
            output [3:0] y);

   wire [3:0] low, high;

   mux2 lowmux(d0, d1, s[0], low);
   mux2 highmux(d2, d3, s[0], high);
   mux2 finalmux(low, high, s[1], y);
endmodule
```

Structural modelling: 4:1 multiplexer

```
module mux4(input [3:0] d0, d1, d2, d3,
            input [1:0] s,
            output [3:0] y);

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   mux2 lowmux(d0, d1, s[0], low);
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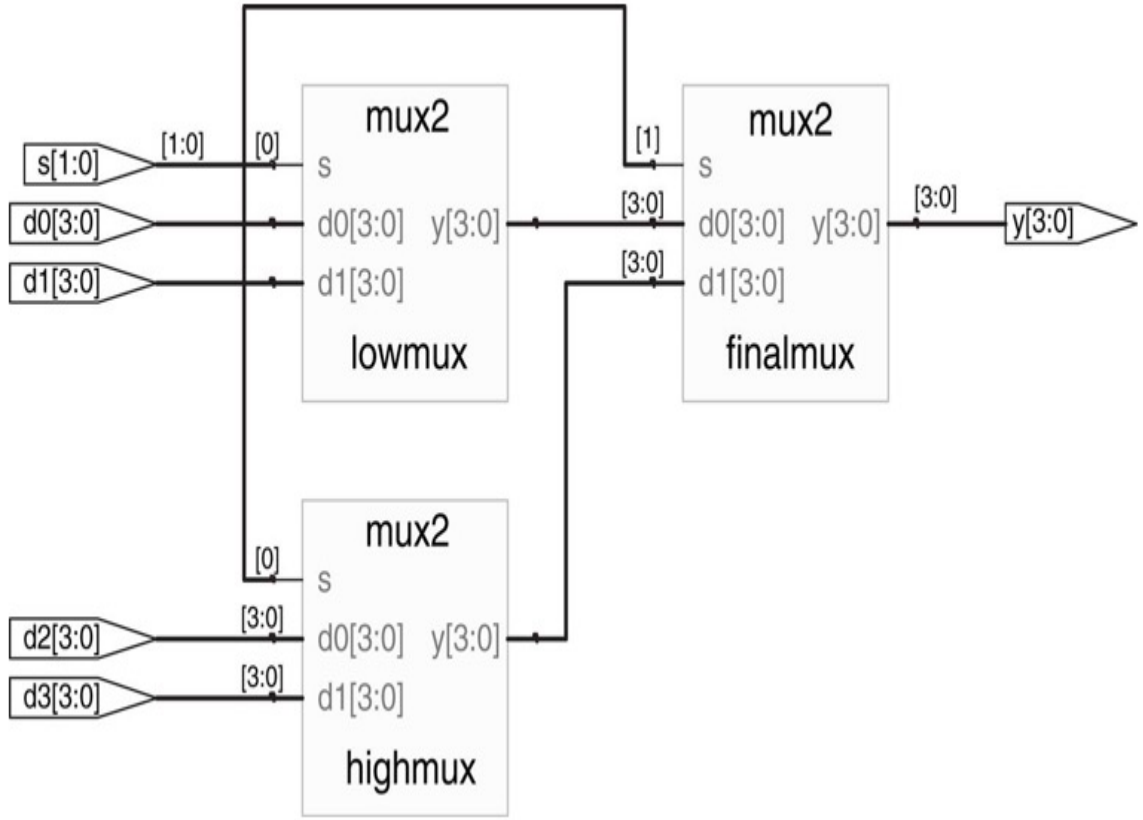
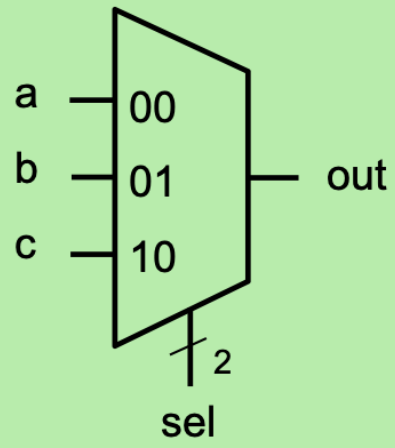
   mux2 finalmux(low, high, s[1], y);
endmodule
```



Dangers of Verilog: Incomplete specification

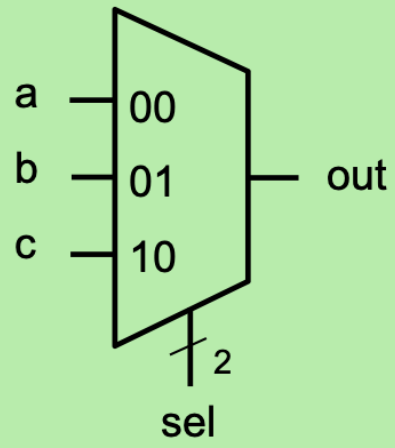
Intended design



3-to-1 MUX
('11' input is a don't-care)

Dangers of Verilog: Incomplete specification

Intended design



3-to-1 MUX
('11' input is a don't-care)

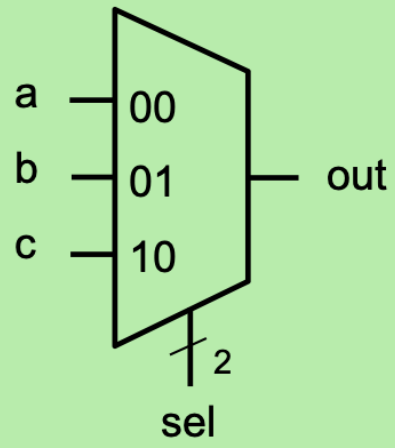
Written Verilog Code:

```
module mux3(input a, b, c,
            input [1:0] sel,
            output out);
reg out_;
assign out = out_;
always@(a or b or c or sel)
begin
        case (sel)
           2'b00: out_ = a;
           2'b01: out_ = b;
           2'b10: out_ = c;
        endcase
end

endmodule
```

Dangers of Verilog: Incomplete specification

Intended design



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        case (sel)
           2'b00: out_ = a;
           2'b01: out_ = b;
           2'b10: out_ = c;
        endcase
end

endmodule
```
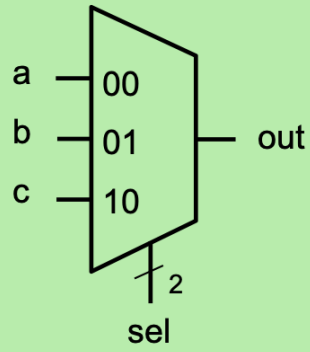

Is this a 3-1 multiplexer?

Dangers of Verilog: Incomplete specification

Intended design



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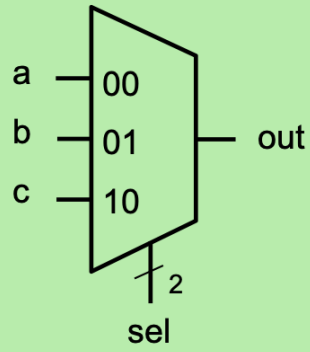
Dangers of Verilog: Incomplete specification

Intended design



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Written Verilog Code:

```
module mux3(input a, b, c,
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reg out_
assign out = out_
always@(a or b or c or sel)
begin
       case (sel)
          2'b00: out_ = a;
          2'b01: out_ = b;
          2'b10: out_ = c;
       endcase
end
endmodule
```
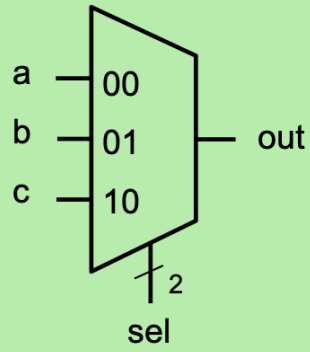

Dangers of Verilog: Incomplete specification

Intended design



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begin
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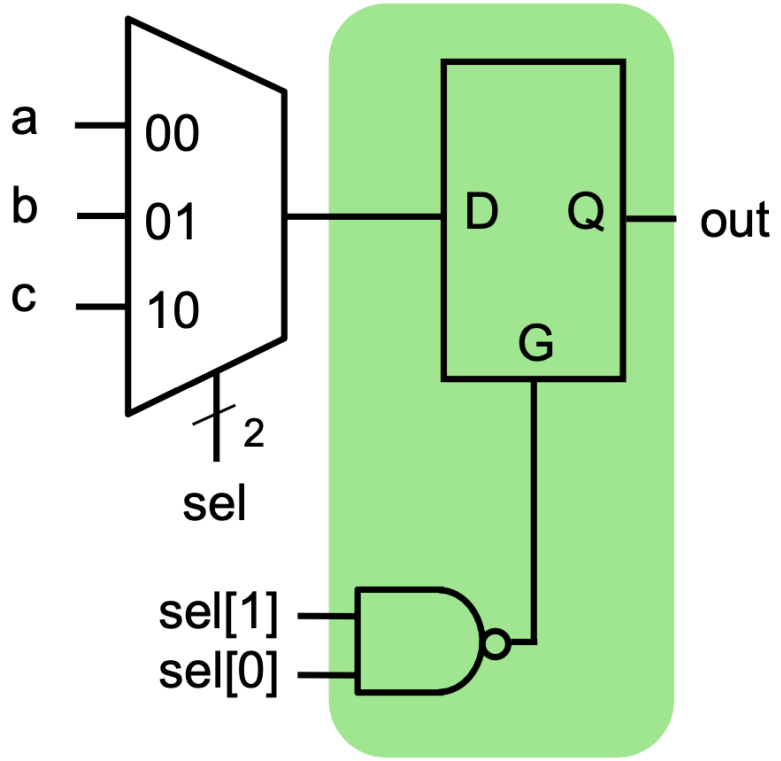
            2'b00: out_ = a;
            2'b01: out_ = b;
            2'b10: out_ = c;
        endcase
end
endmodule
```

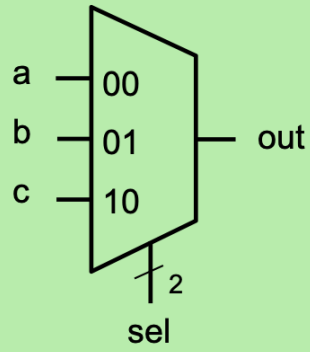
Synthesized result



if `out` is not assigned during any pass through the always block, then the previous value must be retained!

Dangers of Verilog: Incomplete specification

Intended design

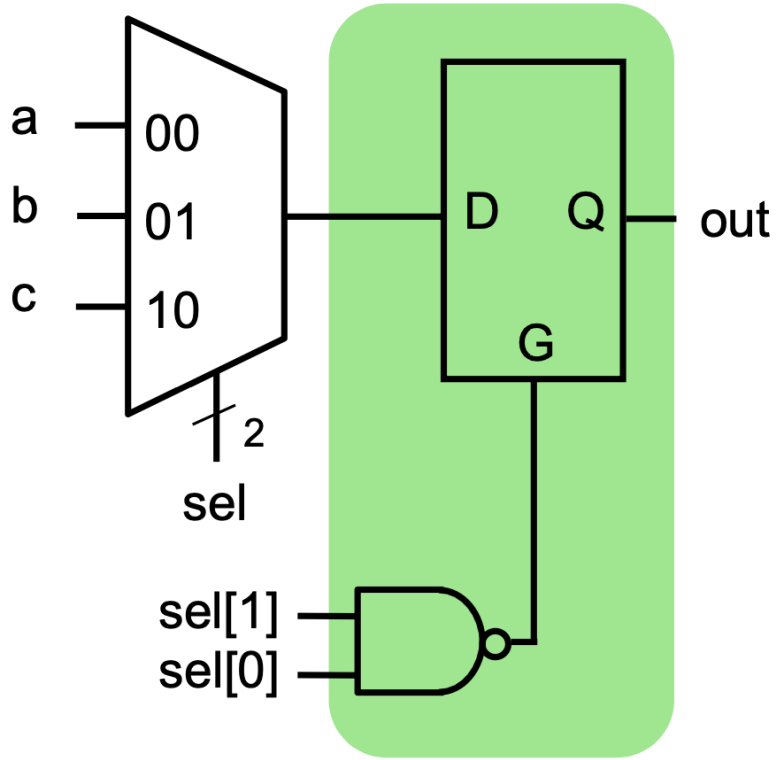


3-to-1 MUX
('11' input is a don't-care)

Written Verilog Code:

```
module mux3(input a, b, c,
            input [1:0] sel,
            output out);
reg out_
assign out = out_
always@(a or b or c or sel)
begin
        case (sel)
            2'b00: out_ = a;
            2'b01: out_ = b;
            2'b10: out_ = c;
        endcase
end
endmodule
```

Synthesized result



if `out` is not assigned during any pass through the always block, then the previous value must be retained!

Latch memory "latches" old data when G=0

Avoiding incomplete specification

```
always@(a or b or c or sel)
begin
        out_ = 1'bx;
        case (sel)
           2'b00: out_ = a;
           2'b01: out_ = b;
           2'b10: out_ = c;
        endcase
end
```

Avoiding incomplete specification

- **Precede all conditionals with a default assignment for all signals assigned within them...**

```
always@(a or b or c or sel)
begin
        out_ = 1'bx;
        case (sel)
           2'b00: out_ = a;
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           2'b10: out_ = c;
        endcase
end
```

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always@(a or b or c or sel)
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           2'b00: out_ = a;
           2'b01: out_ = b;
           2'b10: out_ = c;
           default: out_ = 1'bx;
        endcase
end
```

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```
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        out_ = 1'bx;
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           2'b00: out_ = a;
           2'b01: out_ = b;
           2'b10: out_ = c;
        endcase
end
```

- **...or, fully specify all branches of conditionals and assign all signals from all branches**

For each `if`, include `else` For each `case`, include `default`

```
always@(a or b or c or sel)
begin
        case (sel)
           2'b00: out_ = a;
           2'b01: out_ = b;
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           default: out_ = 1'bx;
        endcase
end
```
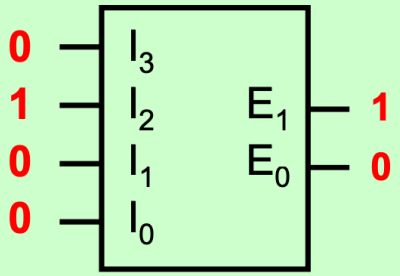

Dangers of Verilog: Priority logic

Intended design

4-to-2 Binary Encoder

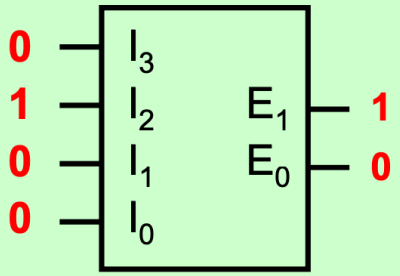


I_3 I_2 I_1 I_0	E_1 E_0
0 0 0 1	0 0
0 0 1 0	0 1
0 1 0 0	1 0
1 0 0 0	1 1
all others	X X

Dangers of Verilog: Priority logic

Intended design

4-to-2 Binary Encoder



I_3 I_2 I_1 I_0	E_1 E_0
0 0 0 1	0 0
0 0 1 0	0 1
0 1 0 0	1 0
1 0 0 0	1 1
all others	X X

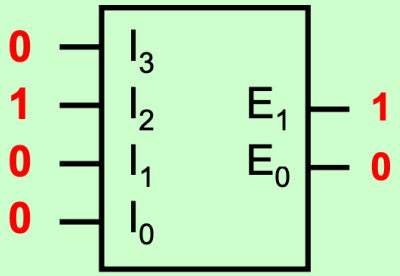
Written Verilog Code:

```
module encoder(input [3:0]i,
                    output [1:0] e);
        reg [1:0]e_;
        assign e<=e_;
always @(i)
begin
        if (i[0]) e = 2'b00;
        else if (i[1]) e_ = 2'b01;
        else if (i[2]) e_ = 2'b10;
        else if (i[3]) e_ = 2'b11;
        else e_ = 2'bxx;
end
endmodule
```

Dangers of Verilog: Priority logic

Intended design

4-to-2 Binary Encoder



I_3 I_2 I_1 I_0	E_1 E_0
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0 0 1 0	0 1
0 1 0 0	1 0
1 0 0 0	1 1
all others	X X

Written Verilog Code:

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module encoder(input [3:0]i,
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begin
        if (i[0]) e = 2'b00;
        else if (i[1]) e_ = 2'b01;
        else if (i[2]) e_ = 2'b10;
        else if (i[3]) e_ = 2'b11;
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```

What is the resulting circuit?

Dangers of Verilog: Priority logic

Intent: **if more than one input is 1, the result is a don't-care.**

I_3 I_2 I_1 I_0	E_1 E_0
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0 0 1 0	0 1
0 1 0 0	1 0
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1 0 0 0	1 1
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Code: **if i[0] is 1, the result is 00 regardless of the other inputs.** ***i[0] takes the highest priority.***

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if (i[0]) e = 2'b00;
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end
```

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0 0 1 0	0 1
0 1 0 0	1 0
1 0 0 0	1 1
all others	X X

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if (i[0]) e = 2'b00;
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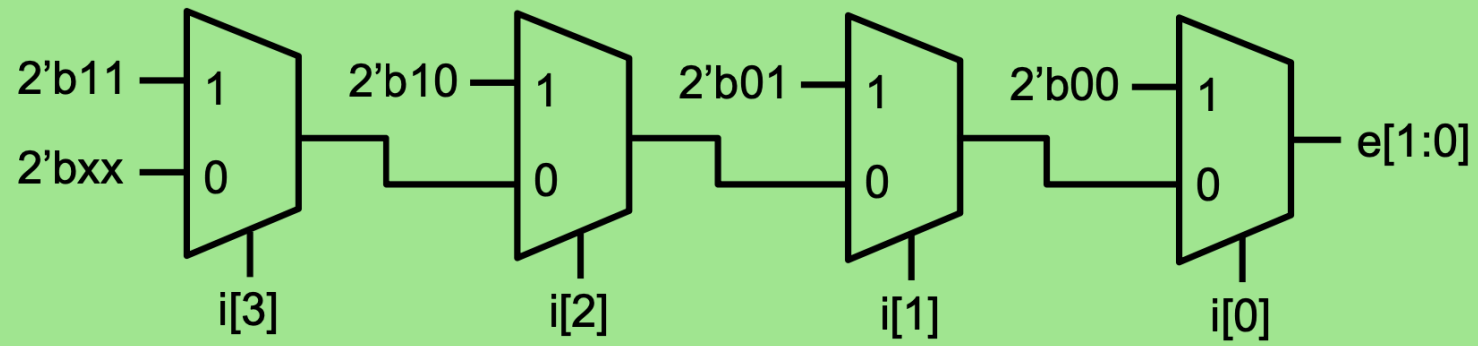
end
```

Inferred Result:



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1 0 0 0	1 1
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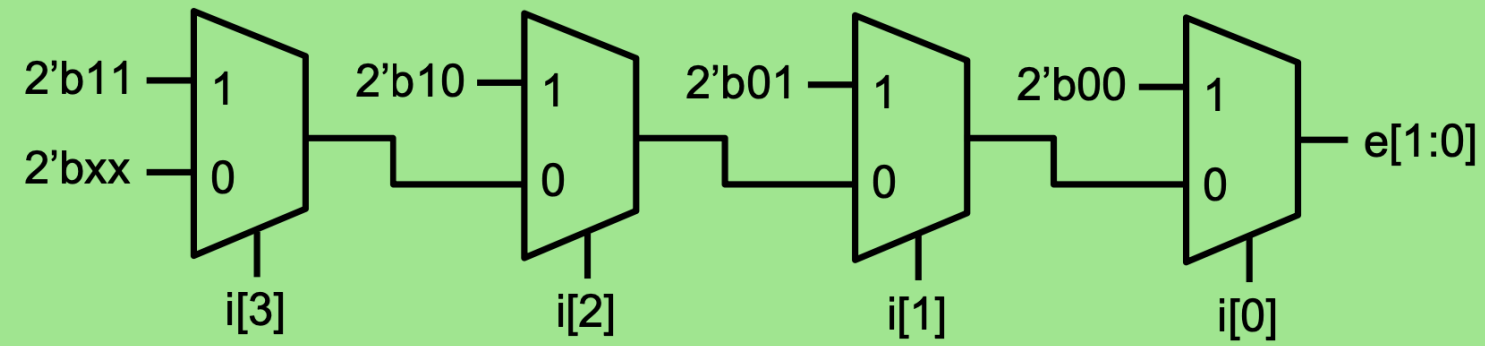

`if-else` **and** `case` **statements are interpreted literally! Beware of unintended priority logic.**

Avoiding unintended priority logic

Make sure that if-else and case statements are *parallel*

If mutually exclusive conditions are chosen for each branch...

...then synthesis tool can generate a simpler circuit that evaluates the branches in parallel

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Parallel Code:

```
module encoder(input [3:0]i,
               output [1:0] e);
       reg [1:0]e_;
       assign e<=e_;
always @(i)
begin
       if (i = 4'b0001) e = 2'b00;
       else if (i = 4'b0010) e_ = 2'b01;
       else if (i = 4'b0100) e_ = 2'b10;
       else if (i = 4'b1000) e_ = 2'b11;
       else e_ = 2'bxx;
end
endmodule
```

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always @(i)
begin
       if (i = 4'b0001) e = 2'b00;
       else if (i = 4'b0010) e_ = 2'b01;
       else if (i = 4'b0100) e_ = 2'b10;
       else if (i = 4'b1000) e_ = 2'b11;
       else e_ = 2'bxx;
end
endmodule
```
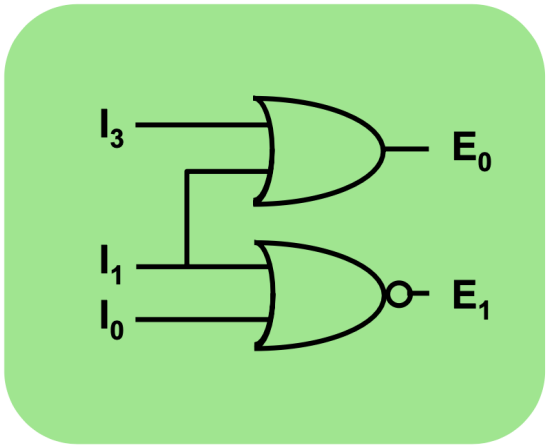

Minimized synthesis result



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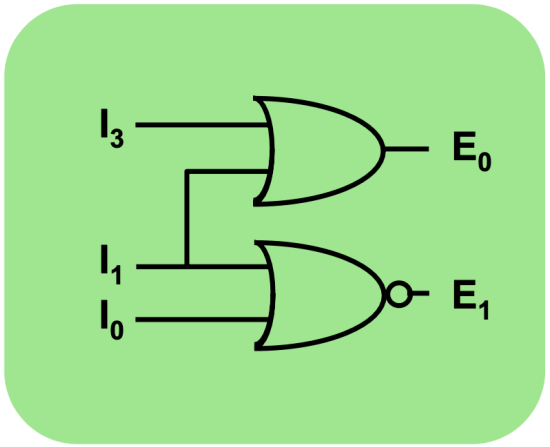
               output [1:0] e);
       reg [1:0]e_;
       assign e<=e_;
always @(i)
begin
       if (i = 4'b0001) e = 2'b00;
       else if (i = 4'b0010) e_ = 2'b01;
       else if (i = 4'b0100) e_ = 2'b10;
       else if (i = 4'b1000) e_ = 2'b11;
       else e_ = 2'bxx;
end
endmodule
```

Minimized synthesis result



Optimization

I_3 I_2 I_1 I_0	E_1 E_0
0 0 0 1	0 0
0 0 1 0	0 1
0 1 0 0	1 0
1 0 0 0	1 1
all others	X X

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       reg [1:0]e_;
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begin
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       else if (i = 4'b0010) e_ = 2'b01;
       else if (i = 4'b0100) e_ = 2'b10;
       else if (i = 4'b1000) e_ = 2'b11;
       else e_ = 2'bxx;
end
endmodule
```
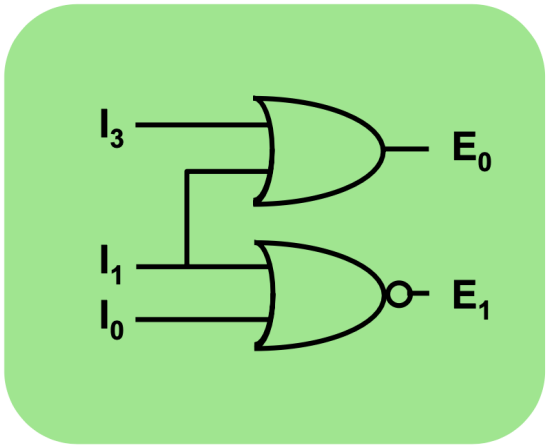

Minimized synthesis result



Why I_2 is missing?

Optimization

I_3 I_2 I_1 I_0	E_1 E_0
0 0 0 1	0 0
0 0 1 0	0 1
0 1 0 0	1 0
1 0 0 0	1 1
all others	X X

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Parallel Code:

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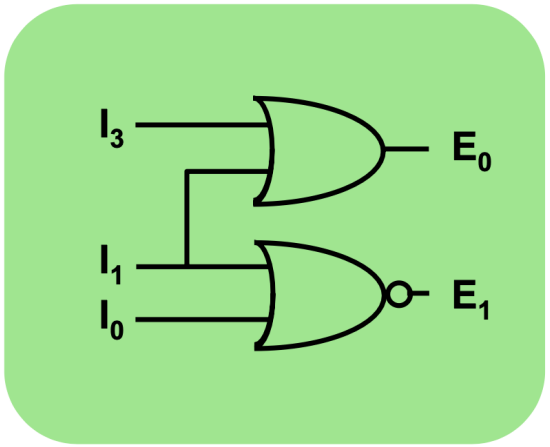
               output [1:0] e);
       reg [1:0]e_;
       assign e<=e_;
always @(i)
begin
       if (i = 4'b0001) e = 2'b00;
       else if (i = 4'b0010) e_ = 2'b01;
       else if (i = 4'b0100) e_ = 2'b10;
       else if (i = 4'b1000) e_ = 2'b11;
       else e_ = 2'bxx;
end
endmodule
```

Minimized synthesis result



Why I_2 is missing?

Optimization

I_3 I_2 I_1 I_0	E_1 E_0
0 0 0 1	0 0
0 0 1 0	0 1
0 1 0 0	1 0
1 0 0 0	1 1
all others	X X

E_0 =1 when only I_1 or I_3 is 1

E_1 =1 when both I_0 and I_1 are 0

Avoiding unintended priority logic

Make sure that if-else and case statements are *parallel*

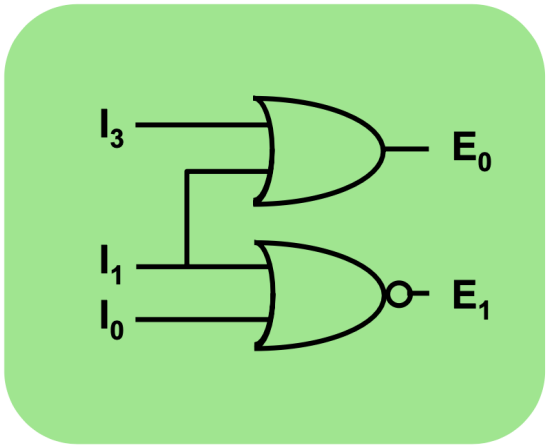
If mutually exclusive conditions are chosen for each branch...

...then synthesis tool can generate a simpler circuit that evaluates the branches in parallel

Parallel Code:

```
module encoder(input [3:0]i,
               output [1:0] e);
       reg [1:0]e_;
       assign e<=e_;
always @(i)
begin
       if (i = 4'b0001) e = 2'b00;
       else if (i = 4'b0010) e_ = 2'b01;
       else if (i = 4'b0100) e_ = 2'b10;
       else if (i = 4'b1000) e_ = 2'b11;
       else e_ = 2'bxx;
end
endmodule
```

Minimized synthesis result



Why I_2 is missing?

Optimization

I_3 I_2 I_1 I_0	E_1 E_0
0 0 0 1	0 0
0 0 1 0	0 1
0 1 0 0	1 0
1 0 0 0	1 1
all others	X X

E_0 =1 when only I_1 or I_3 is 1

E_1 =1 when both I_0 and I_1 are 0

Therefore, I_2 can be safely optimized

Delays

```
module example(input a, b, c,
               output y);
  wire ab, bb, cb, n1, n2, n3;
  assign #1 {ab, bb, cb} = ~{a, b, c};
  assign #2 n1 = ab & bb & cb;
  assign #2 n2 = a & bb & cb;
  assign #2 n3 = a & bb & c;
  assign #4 y = n1 | n2 | n3;
endmodule
```

Delays

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- The delay for each assignment is specified: time between change of input and update of output.
- Delays are for simulation only! They do not determine the delay of the circuit after synthesis.

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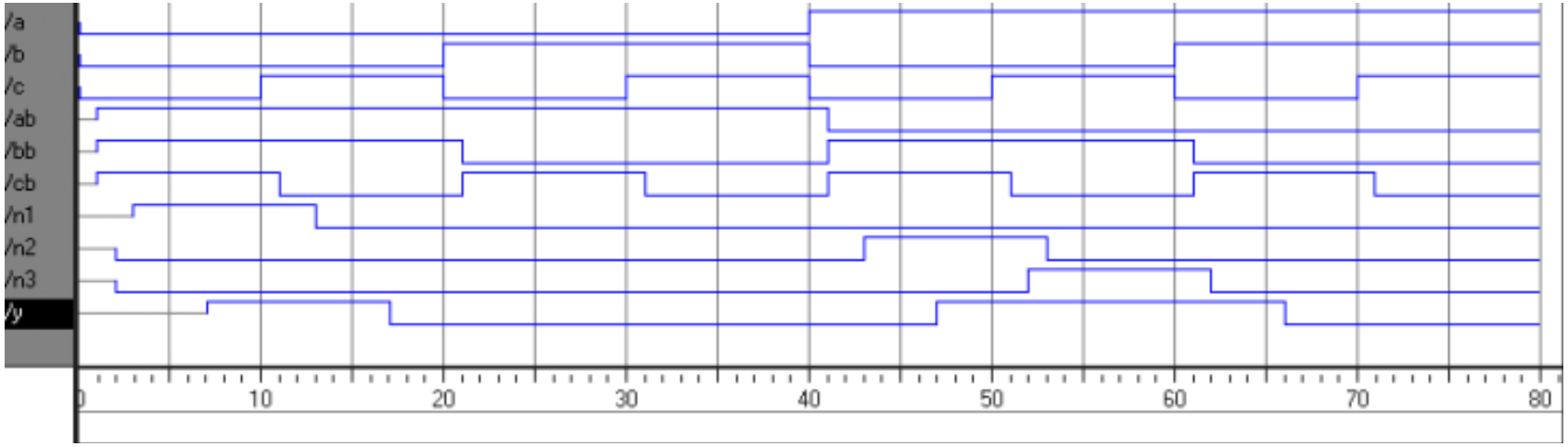
Simulation



Delays

Updates triggered by events on a, b, c

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module example(input a, b, c,
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endmodule
```
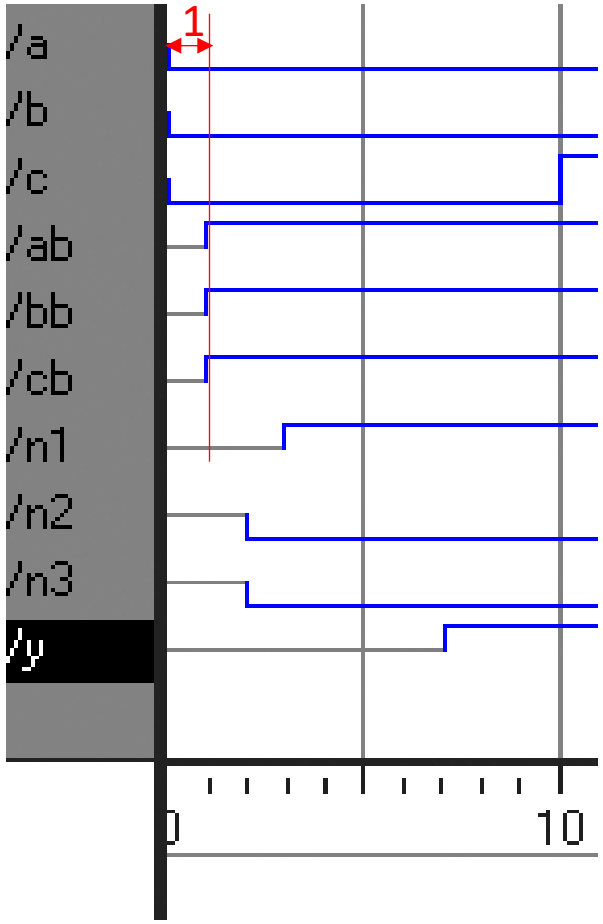

Simulation



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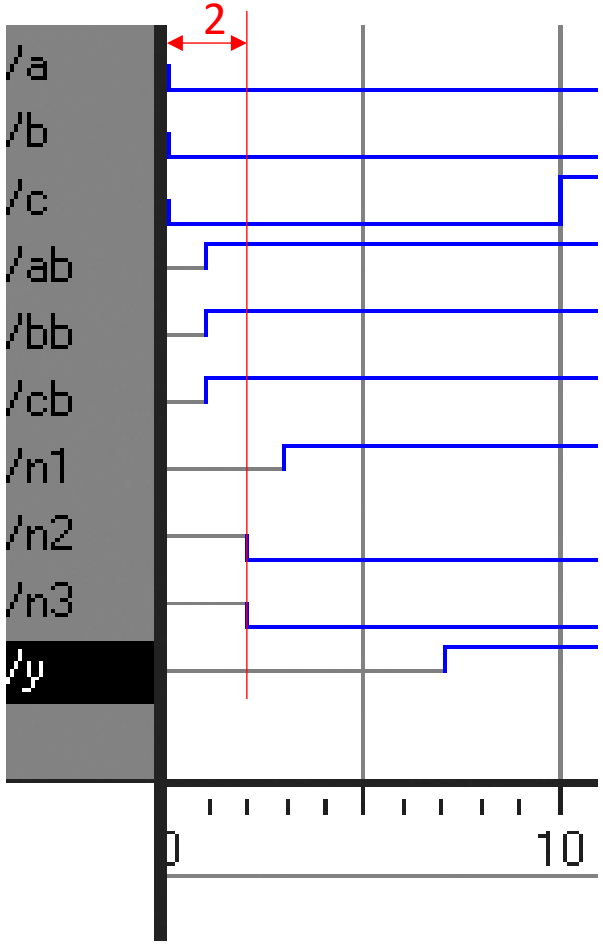
Simulation



Delays

Update triggered by events on ab, bb, cb

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module example(input a, b, c,
               output y);
  wire ab, bb, cb, n1, n2, n3;
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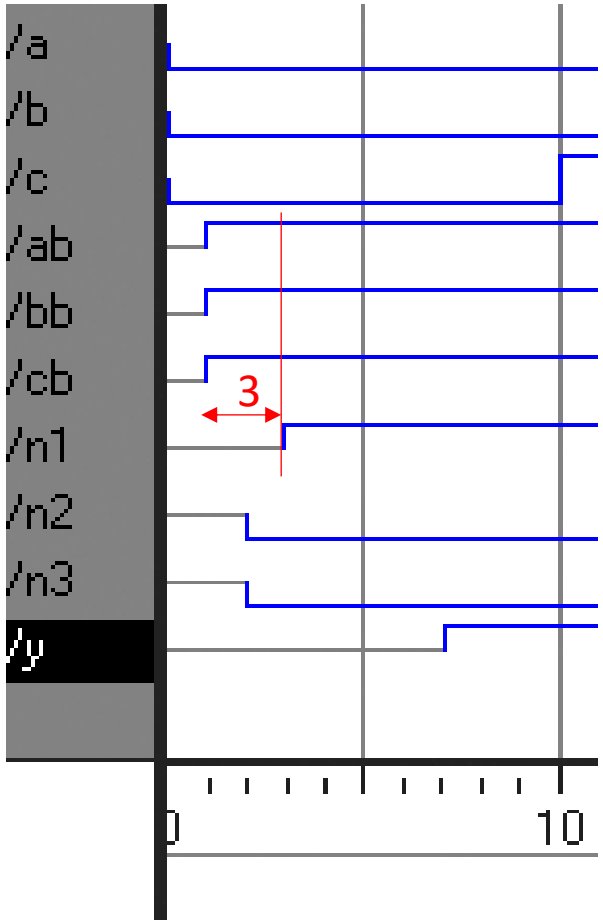
```

Simulation

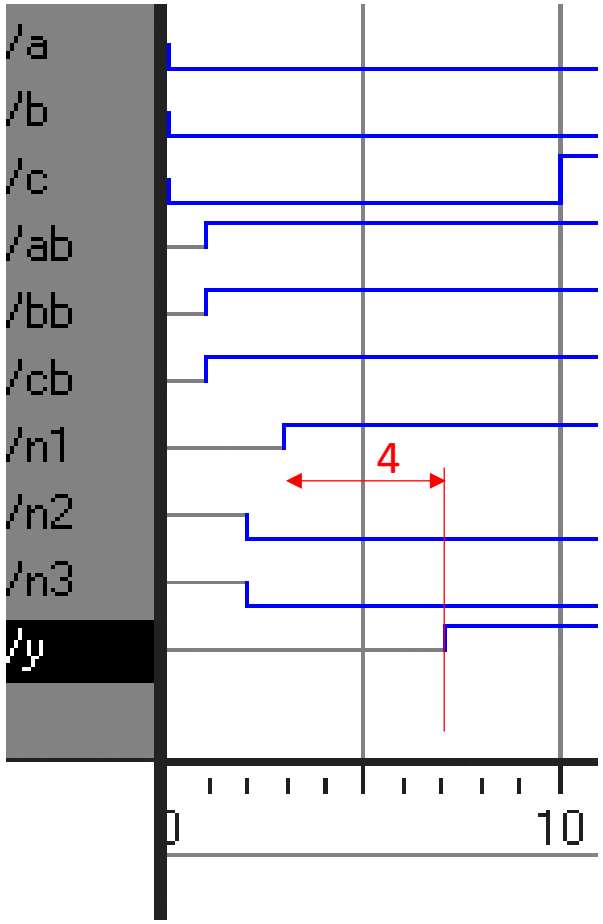


Delays

Update triggered by event on n1

```
module example(input a, b, c,
               output y);
  wire ab, bb, cb, n1, n2, n3;
  assign #1 {ab, bb, cb} = ~{a, b, c};
  assign #3 n1 = ab & bb & cb;
  assign #2 n2 = a & bb & cb;
  assign #2 n3 = a & bb & c;
  assign #4 y = n1 | n2 | n3;
endmodule
```

Simulation



Verilog simulation & synthesis

```
module example(input a, b, c,
               output y);
   assign y = ~a & ~b & ~c | a & ~b & ~c | a & ~b &  c;
endmodule
```

Verilog simulation & synthesis

```
module example(input a, b, c,
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   assign y = ~a & ~b & ~c | a & ~b & ~c | a & ~b &  c;
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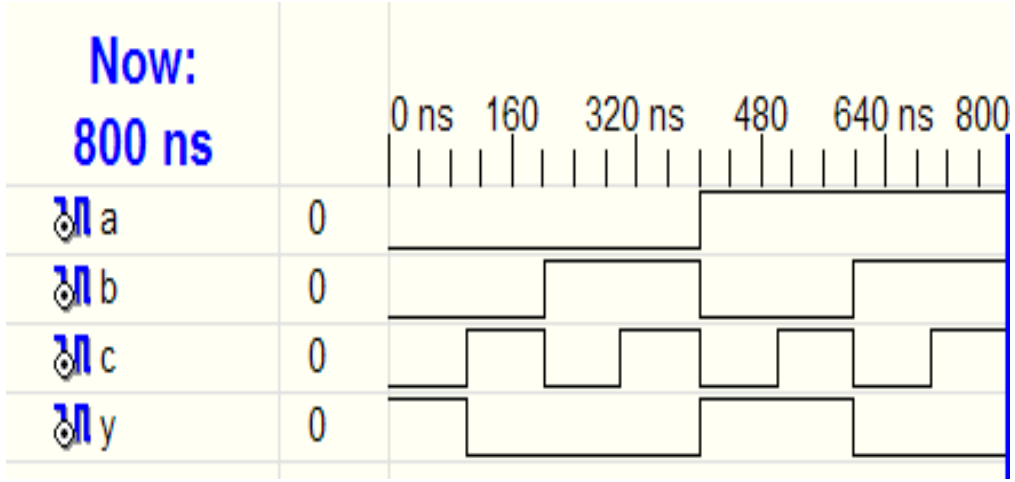
```

Simulation Results



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module example(input a, b, c,
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   assign y = ~a & ~b & ~c | a & ~b & ~c | a & ~b &  c;
endmodule
```
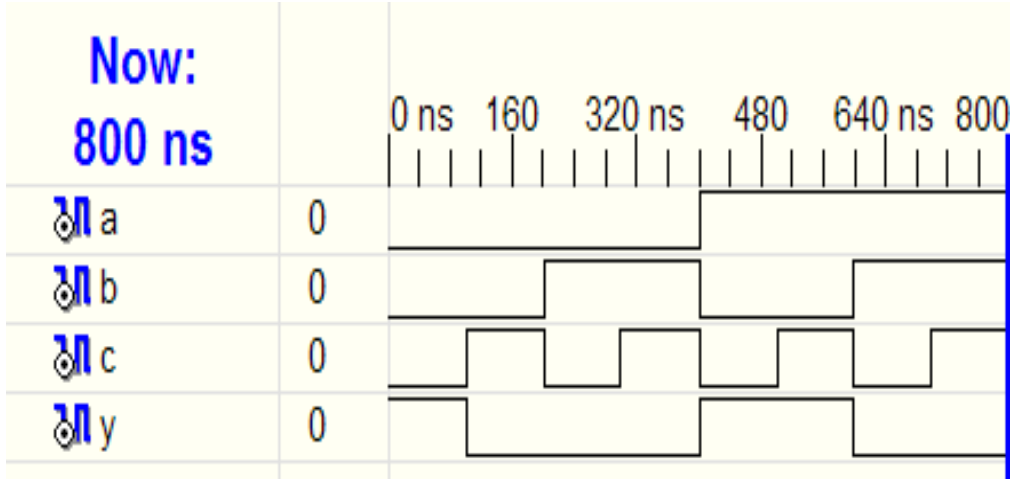
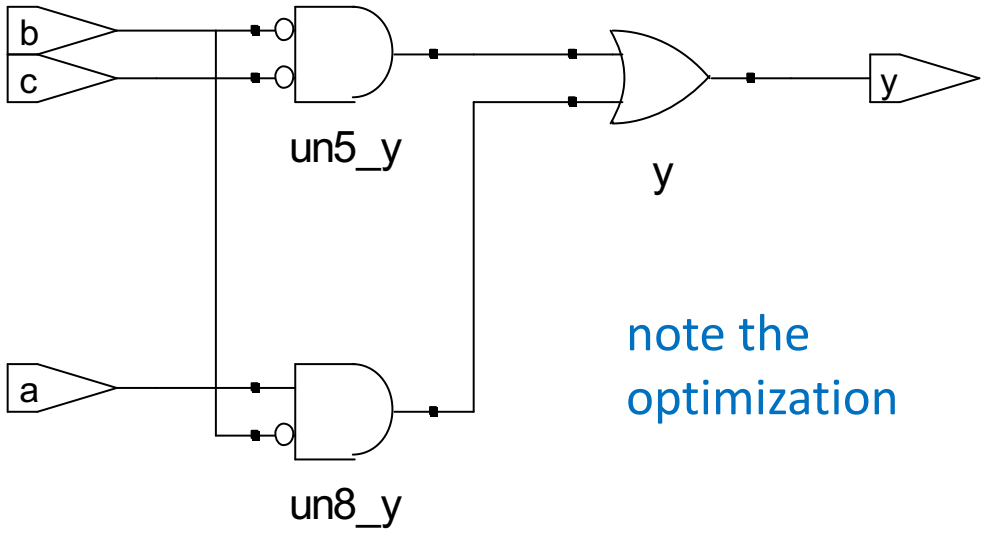

Simulation Results



Synthesis Results



note the optimization

Verilog testbenches

- HDL module that **tests another module**: *device under test* (dut)

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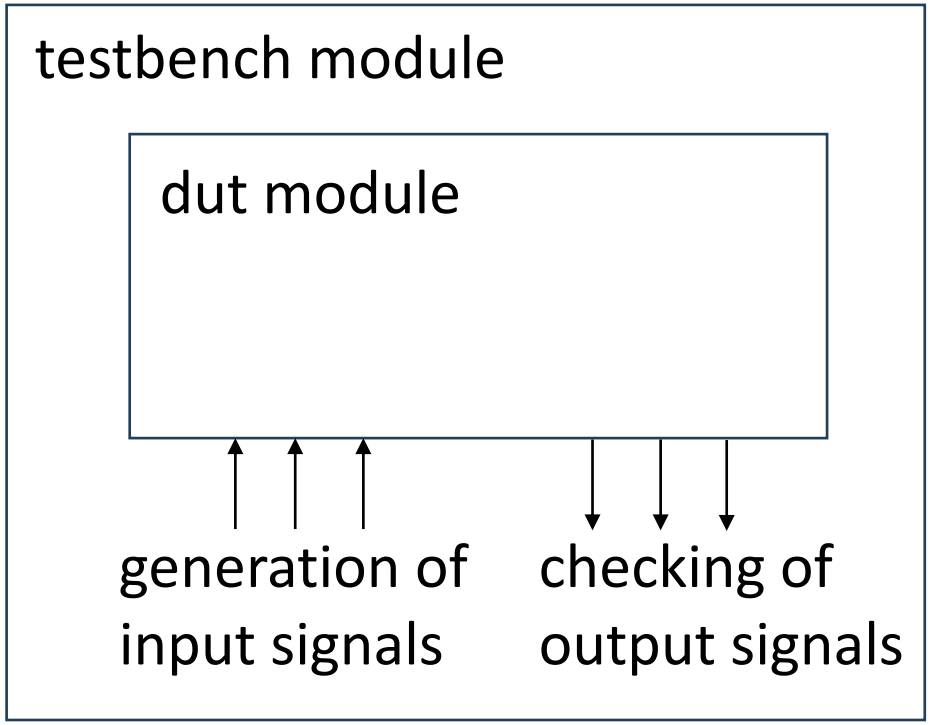
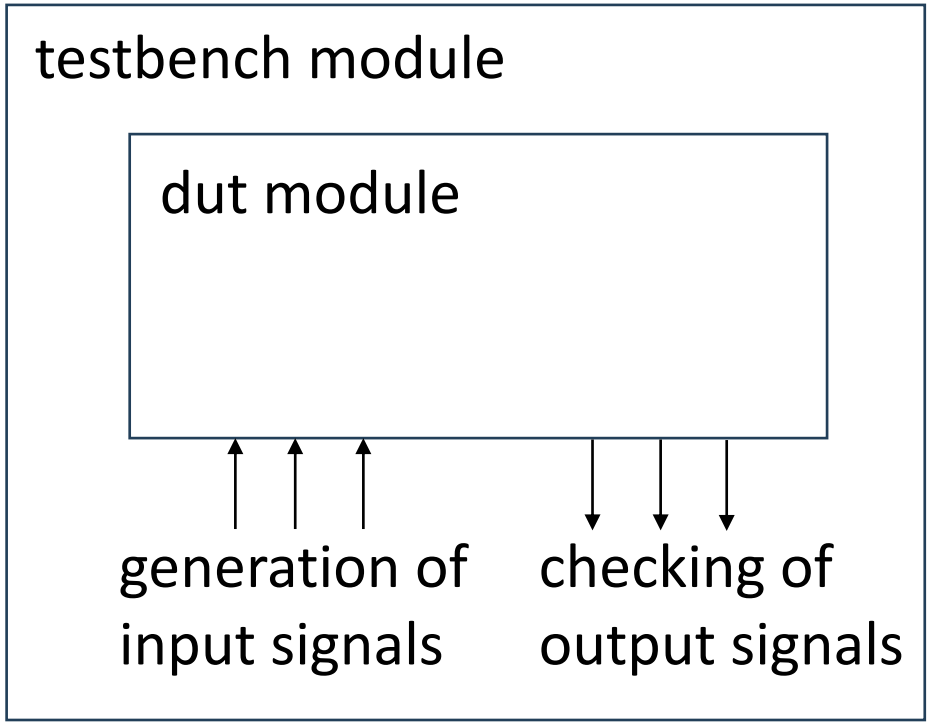


Verilog testbenches

- HDL module that **tests another module**: *device under test* (dut)
- **Not synthesizable**
- **Types:**
  - Simple
  - Self-checking



Testbenches

Write Verilog code to implement the following function in hardware. Name the module **`myfunction`**.

`y = bc + ab`

```
module myfunction(input a, b, c,
                  output y);
  assign y = ~b & ~c | a & ~b;
endmodule
```

Testbench 1: Simple testbench

```
module tb1();
```

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module tb1();
  reg a, b, c;
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module tb1();
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  myfunction dut(a, b, c, y);
  // apply new set of inputs every 10 time-units
  initial begin
    a = 0; b = 0; c = 0; #10; //apply inputs, wait 10ns
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           b = 1; c = 0; #10; //change the values of b & c, wait 10ns
```

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    a = 0; b = 0; c = 0; #10; //apply inputs, wait 10ns
                  c = 1; #10; //change the value of c, wait 10ns
           b = 1; c = 0; #10; //change the values of b & c, wait 10ns
                  c = 1; #10; //etc
    a = 1; b = 0; c = 0; #10;
                  c = 1; #10;
           b = 1; c = 0; #10;
                  c = 1; #10;
  end
endmodule
```
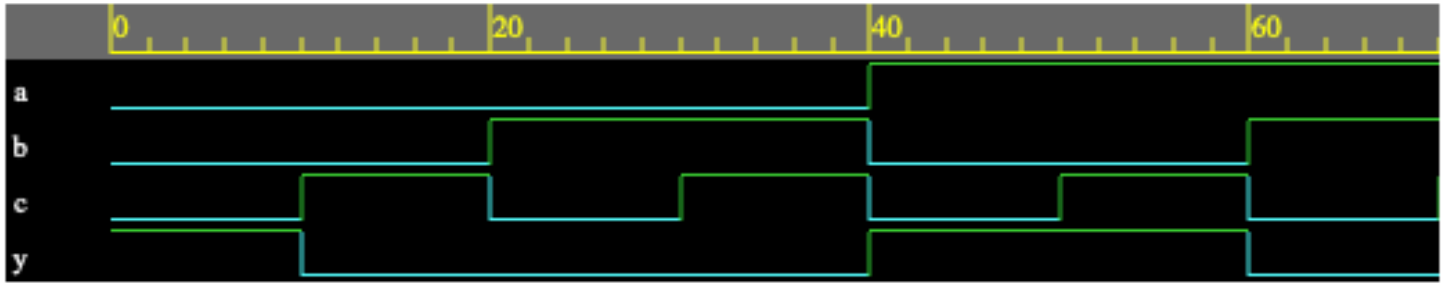

Simulation result

```
module tb1();
  reg a, b, c;
  wire y;
  // instantiate device under test
  myfunction dut(.a(a), .b(b), .c(c), .y(y));
  // apply new set of inputs every 10 time-units
  initial begin
    a = 0; b = 0; c = 0; #10; //apply inputs, wait 10ns
                  c = 1; #10; //change the value of c, wait 10ns
           b = 1; c = 0; #10; //change the values of b & c, wait 10ns
                  c = 1; #10; //etc
    a = 1; b = 0; c = 0; #10;
                  c = 1; #10;
           b = 1; c = 0; #10;
                  c = 1; #10;
  end
endmodule
```



Testbench 2: Self-checking testbench

```
module tb2();
  reg  a, b, c;
  wire y;
  // instantiate dut
  myfunction dut(.a(a), .b(b), .c(c), .y(y));
  // apply inputs, check results one at a time
  initial begin
    a = 0; b = 0; c = 0; #10;  if (y !== 1) $display("000 failed.");
                   c = 1; #10;  if (y !== 0) $display("001 failed.");
           b = 1; c = 0; #10;  if (y !== 0) $display("010 failed.");
                   c = 1; #10;  if (y !== 0) $display("011 failed.");
    a = 1; b = 0; c = 0; #10;  if (y !== 1) $display("100 failed.");
                   c = 1; #10;  if (y !== 1) $display("101 failed.");
           b = 1; c = 0; #10;  if (y !== 0) $display("110 failed.");
                   c = 1; #10;  if (y !== 0) $display("111 failed.");
  end
endmodule
```

Thank you